DEVELOPMENT OF A THIN-FILM SPACE-CHARGE-LIMITED TRIODE

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FOREWORD

This report was prepared by the Solid State Research Center, HUGHES AIRCRAFT COMPANY, Newport Beach, California, on National Aeronautics and Space Administration Contract NAS 12-5 "Development of a Thin-Film Space-Charge-Limited Triode". This work was administered in the Electronic Research Center of NASA, Cambridge, Massachusetts, under the direction of Mr. J. Lowen.

This report describes the development effort and the electrical evaluation of a thin-film space-charge-limited triode begun in March 1965 and concluded in June 1966 by the Solid State Research Center of HUGHES AIRCRAFT COMPANY. The principal investigator of the contract studies was Mr. R. Zuleeg and the authors of this report are Mr. R. Zuleeg and Dr. P. Knoll. Others who contributed to the work reported on, are: Mr. R. J. Belardi, Mrs. A. P. Brown, Mr. N. Nicolson, Mr. F. A. Rhoads, Mr. J. F. Ryan, Miss E. J. Senkovits, Mr. M. Siracusa, and Mr. R. P. Totah.

This report was submitted June 1966.

PROGRAM OBJECTIVES

The objective of this contract was to develop a practical thin-film space-charge-limited triode based upon the theoretical concepts of G. T. Wright, which were published in the Proceedings of the IEEE, November 1963, pp. 1642-1652 under the title "Space-Charge-Limited Solid-State Devices".

ABSTRACT

Experimental and theoretical research and development on a thin-film space-charge-limited triode is presented. This includes, experimental results of thin-film CdS-Si and GaAs-Si heterojunction transistors operating under space-charge-limited emitter current; a method to determine the density of states at a heterojunction interface; the design and electrical measurements of a thin-film space-charge-limited triode in the dielectric surface gate structure employing the silicon-on-sapphire technique; the film properties of CdS, GaAs, and Si; correlation of electrical results with the device physics and structure and finally discussion and conclusions based upon the electrical characteristics established with the device structures fabricated.

The limitations of the device structures investigated are assessed with respect to frequency and temperature of operation and the results extrapolated to device structures feasible in the near future by employing improved photolithographic and material technology.

SECTION A

GENERAL DISCUSSION OF SPACE-CHARGE-LIMITED DEVICES AND THEORY

A) GENERAL DISCUSSION OF SPACE-CHARGE-LIMITED DEVICES AND THEORY

Space-charge-limited current is a majority carrier current, when double injection operation is excluded, which leads to nonlinear behavior. The discussion will be concerned only with space-charge-limited devices regarded as a majority carrier device. Since we consider only linear devices, e.g. those with a power gain, a space-charge-limited triode should be defined by, and confined to: a three-terminal semiconductor device, which operates under space-charge-limited current condition, whereby the space-charge-limited current is modulated by means of a high impedance gate or grid. This is to say, the gate terminal essentially does not draw any direct current and exerts only a field-effect control mechanism upon injected majority carriers. These carriers under space-charge-limited condition are presented above the value of the thermally generated carriers in the material under question. The foregoing statement is conditional for space-charge-limited currents, which commence only when the ohmic currents are smaller than the induced space-charge-limited currents in the material. In accordance with this definition of space-charge-limited currents and confining the operation to majority carriers only, the following classes of space-charge-limited solid-state devices can be derived:

Class 1: The devices of this class operate under space-charge-limited conditions over a fixed geometrical distance, L_o. With charge control exerted from a high impedance terminal (= grid or gate) the following general voltage-current characteristics are expected:

$$I_{DRAIN} = \frac{9\varepsilon\varepsilon_o \mu A}{8L_o^3} \left[V_G + \frac{V_D}{G} \right]^2 \tag{1}$$

Class 2: The devices operate under space-charge-limited current conditions over a variable distance $L_v = L_o + L(V_G)$. With charge control exerted from a high impedance terminal (grid or gate) the following general voltage-current characteristics are expected:

$$I_{DRAIN} = \frac{9 \varepsilon \varepsilon_o \mu A V_D^2}{8 \left[L_o + L(V_G) \right]^3} \quad (2)$$

Class 3: The devices operate under space-charge-limited current conditions over a fixed distance L_o. With charge control mechanism from a high impedance terminal (= grid or gate) the cross sectional area A is made variable to the majority carrier flow prior to entering the material carrier space-charge-limited current. The following general voltage-current characteristics are expected:

$$I_{DRAIN} = \frac{9 \varepsilon \varepsilon_o \mu V_D^2}{8 L_o^3} \quad A(V_G) \quad (3)$$

All devices of these three classes show theoretically the characteristic vacuum-tube triode voltage-current relations with exponential power relation, e.g. power of 2 for the ideal solid-state device and power of 3/2 for the ideal vacuum triode.

The ideal device of Class 1 was first proposed by Wright[1] and employs the insertion of a metallic grid or gate between the plane parallel electrodes designated drain and source (see Figure 1a). This device has never been realized in practice, although progressing advances in thin-film material and micro-circuitry technology make this device feasible in the near future. Ion implantation techniques especially could be very advantageous in the construction of such a device.

A modification space-charge-limited triode according to the Class 1 classification, circumventing certain fabrication difficulties of the ideal device as described above, but leading to a somewhat difficult geometry for a theoretical analysis, was successfully demonstrated by Zuleeg[2] and theoretically analyzed by Wright[3]. This thin-film space-charge-limited triode was fabricated in a structure shown in Figure 1b by using polycrystalline CdS. This structure is now feasible in an improved version by employing the silicon-on-sapphire growth technique.

STRUCTURES OF SPACE-CHARGE-LIMITED TRIODES

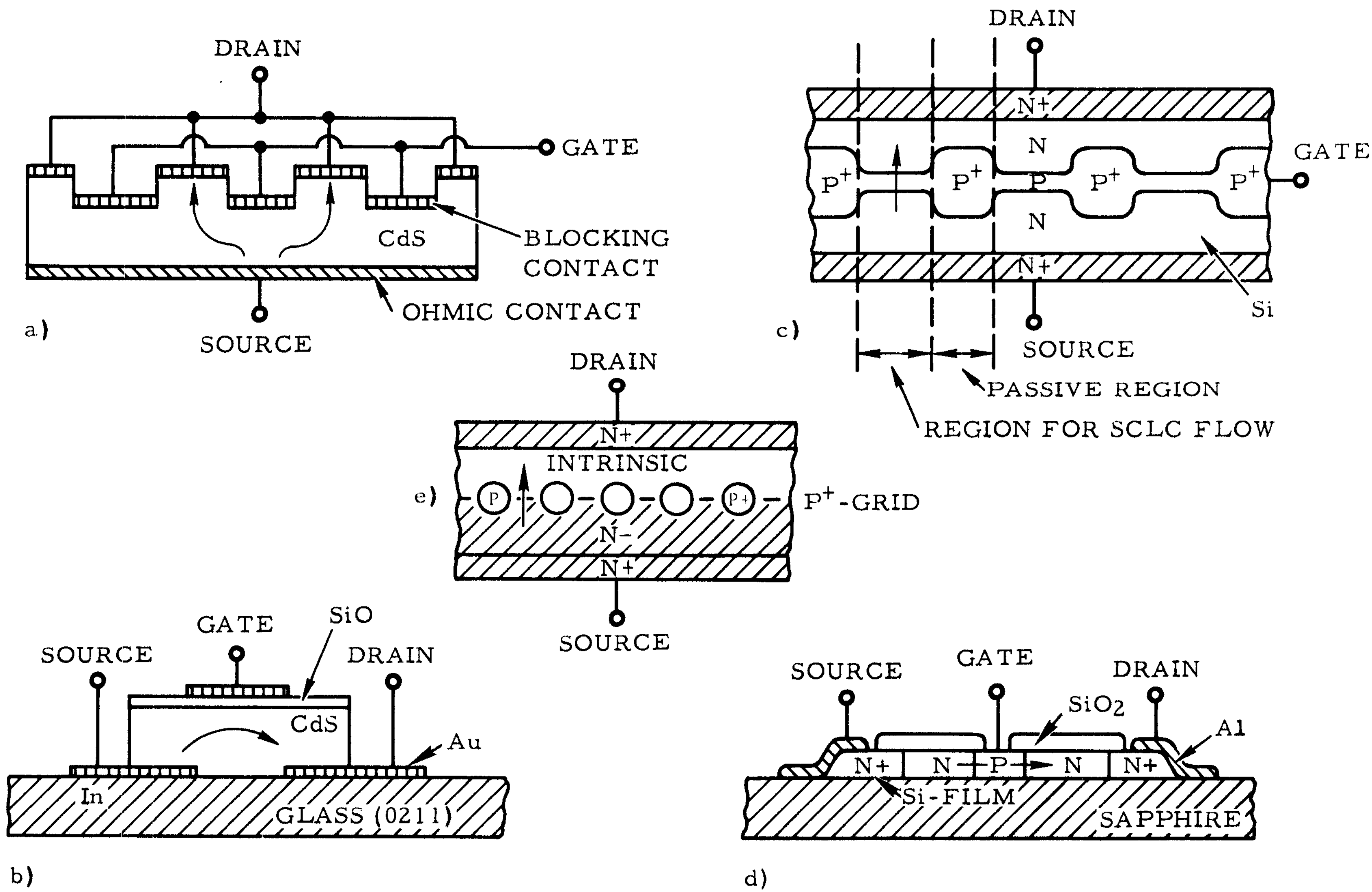


Figure 1

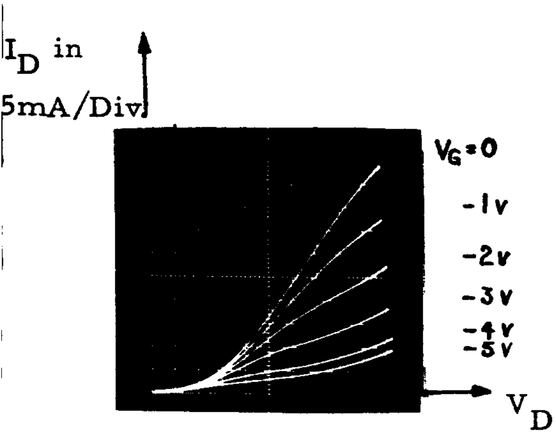
Figure 2 demonstrates a practical structure which was fabricated at the Hughes Solid State Research Center prior to the contract award. This device has been further developed and studied under this contract. The typical triode characteristics of such a device with a transconductance of 1,000μ mho is also shown in Figure 2. The structure was investigated in respect to gain and frequency response and holds great promise as a high frequency thin-film device when possible improvements are considered in regard to geometry and material.

A device of Class 2, and the only one fabricated so far in monolithic construction, was fabricated also at the Hughes Solid State Research Center and described by Zuleeg[4]. A basic structure of this device, which possesses a spatially extended multi-element grid structure in the solid, imposed between two, plane parallel electrodes, designated source and drain is shown in Figure 1c. This device is very promising in respect to low-noise amplification properties[5], but cannot be easily adapted to thin-film fabrication methods. It is primarily a bulk device. One possible thin-film structure is shown in Figure 1d, which could be made by using the silicon-on-sapphire technique, but considerable improvement in the crystal perfection of the silicon film grown by heteroepitaxy has to be accomplished before an attempt in fabrication can be made. A device belonging to Class 3 was described by Shockley[6] but no experimental construction was reported. The basic structure of this device is shown in Figure 1e.

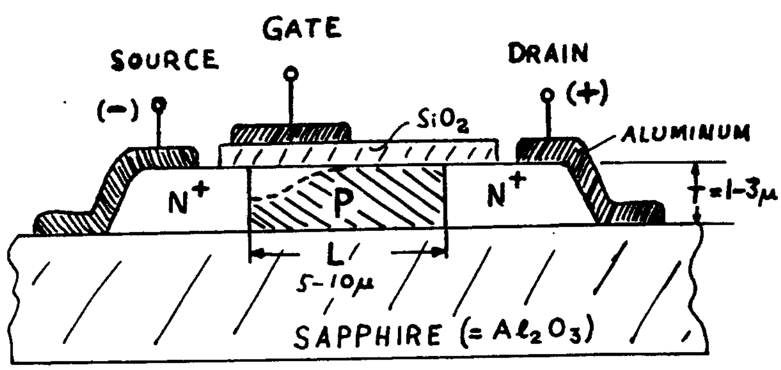
The space-charge-limited dielectric triode, with actual pentode-like characteristic, as proposed by Wright[7] is a mis-nomer and should correctly be called a heterojunction or wide-gap emitter transistor operating under space-charge-limited emitter current condition. Experimental results on this heterojunction transistor employing a CdS-Si junction have been published by Wright[8] and Page[9]. The heterojunction transistor characteristics with a CdS-Si and with a GaAs-Si heterojunction are reported and discussed in this final report. Both heterojunction devices should be placed into the category of the bipolar transistor, since majority and minority carriers are contributing to satisfactory operation of the device. Only in the ideal case, with no recombination at the heterojunction interface due to states, e.g. injection efficiency equal to unity, and no recombination losses of injected minority carriers in the base region during transport, e.g. transport efficiency equal to unity, could one claim a majority

SILICON-ON-SAPPHIRE

SPACE-CHARGE-LIMITED THIN-FILM TRIODE



V_D in 5V/DIV.



TRIODE STRUCTURE

Figure 2

carrier device and classification as a space-charge-limited triode. In all practical cases this device structure will manifest a bipolar transistor operational mechanism with finite base current flow. It should therefore be treated as a normal PN-junction transistor and as a current amplifier, rather than a high input impedance voltage amplifier.

SECTION B

THE HETEROJUNCTION TRANSISTOR

B) THE HETEROJUNCTION TRANSISTOR

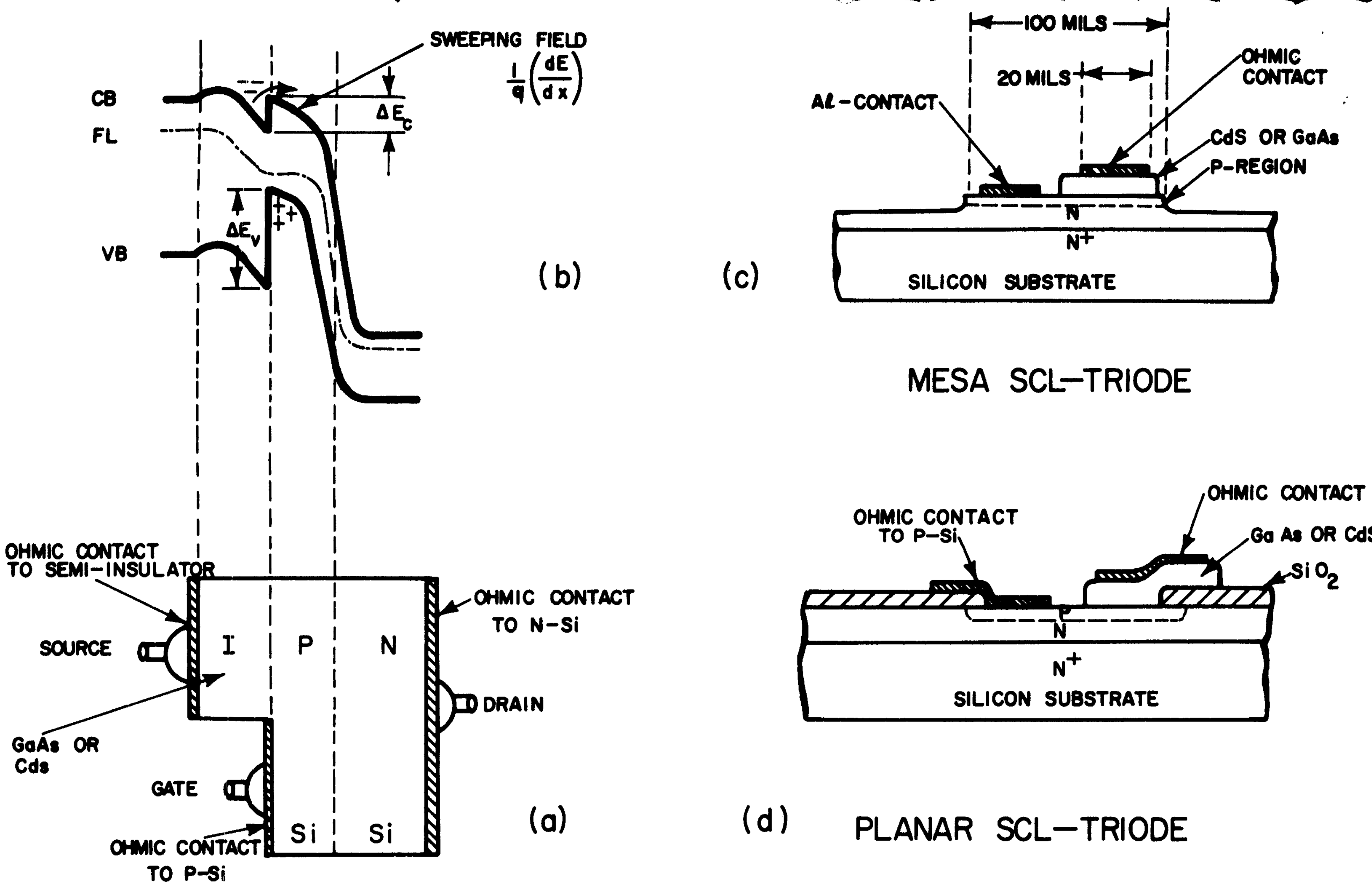
1) CdS-Si Heterojunction Transistor

The space-charge-limited triode first investigated under this contract was proposed by Wright[(7) (3)]. Advantageously it uses a heterojunction gate for charge control exertion and achieves non-reciprocal carrier transmission. In the ideal case, with no recombination in the heterojunction gate or at the heterojunction interface, a true majority carrier device would be the result. How close this ideal condition could be met in practice was investigated in the course of this contract and experimental results were correlated with theory.

The physical structure of the space-charge-limited triode is shown in Figure 3a. The substrate on which the devices were constructed consisted of a low resistivity N-type silicon slice, with an epitaxially grown N-type layer of approximately 0.8 to 1.0 Ωcm resistivity and about 4 to 6 microns thick. The ohmic contact to the header was made with a Sb-Sn preform. The N^+, i.e. ohmic contact, served as the drain. A thin, high conductivity P-skin of 0.5 micron depth was produced by diffusion of boron to act as the gate. A thin-film of high resistivity ($> 10^4$ Ωcm), N-type CdS or GaAs was then deposited by evaporation (see Section D). Ohmic contacts to CdS were provided by evaporating a thin layer of indium and alloying at 160°C. The originally used structure is given in Figure 3c, which is a mesa structure and in the course of the development was replaced by the planar structure shown in Figure 3d.

The band structure of the triode is sketched in Figure 3b when the device is biased for normal operation. The conduction band discontinuities at the CdS and GaAs-Si heterojunction, ΔE_c, are estimated to be in the range of 0.4 to 0.6 eV. The nature of the interface, of course can significantly contribute to the actual values of ΔE_c and ΔE_v. If the potential difference between source and gate produces space-charge-limited current, then electrons are injected into the thin gate region which is equivalent to the base-region of a bipolar NPN transistor. This current is equal to:

$$I_G = \frac{9 \varepsilon \varepsilon_o \mu A (V_G - V_o)^2}{8 L^3} \tag{4}$$



Space-Charge-Limited Triode Operation and Design.
(a) Basic Structure of Triode
(b) Energy Band Structure of Triode Under Normal Bias Operation
(c) Mesa Design of Triode
(d) Planar Design of Triode

Figure 3

and is transferred to the high impedance and back-biased drain PN-junction. The drain current is then given by the relation

$$I_D = \alpha I_G \tag{5}$$

where α is defined as the interfacial transmissivity for the electrons through the heterojunction gate. α is usually smaller than one if losses of the electrons arriving at the heterojunction interface or in the diffused P-region occur. Although the probability of hole injection into the wider gap material is theoretically very small because of the large discontinuity in the valence band at the interface and by the electric field in the depletion region between gate and drain, minority carrier action and $\alpha < 1$ can result from recombination of electrons at the heterojunction interface and during transport through the diffused P-region. All these effects may be combined in the parameter α.

Insertion of Equation 4 into Equation 5 yields the drain current in saturation, I_{DS}, equal to

$$I_{DS} = \alpha \frac{9 \varepsilon \varepsilon_o \mu A (V_G - V_o)^2}{8 L^3} \tag{6}$$

which is independent of drain voltage V_D. The high output impedance of this device results from the complete isolation of output from input, because the gate layer provides excellent electrostatic screening of the source-gate region from the gate-drain region.

According to theory then, the device should have a linear gain function, e.g. the transconductance, g_m, is a linear function of the applied gate voltage, V_G. Differentiation of Equation 6 in respect to V_G yields

$$g_m = \frac{d I_{DS}}{d V_G} = \alpha \frac{9 \varepsilon \varepsilon_o \mu A (V_G - V_o)}{4 L^3} \tag{7}$$

Space-charge-limited triodes have been fabricated using the CdS-Si heterojunction by employing the mesa structure given in Figure 3c. Other investigations have already reported in the literature on such a device[8] [9]. The devices were mounted on T0-5 headers and electrically evaluated. Figure 4 gives grounded source characteristics resulting from a voltage and a current driving source and a grounded gate characteristic resulting from a current driving source to obtain the actual electron transmissivity. For device N-19 in Figure 4 we obtained $\alpha = 0.8$, which corresponds to a $\beta = 4$ for a bipolar transistor and a transconductance $g_m = 2$ mA/V. The input capacitance of the device, constant and independent of current, was 75 pf so that the calculated gain-bandwidth product is equal to

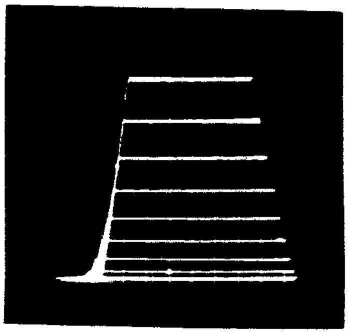
$$G.\ BW = \frac{g_m}{2\pi C_{in}} = 4.2\ \text{MC} \qquad (8)$$

Frequency response measurements indicated a value of 1 to 2 MC.

A plot of $I_{DS}^{1/2}$ vs. V_G in Figure 5 confirms the square law characteristic according to Equation 4. The threshold voltage is about 1 volt and $\alpha = 0.8$. The computed mobility in the CdS film is about 7 cm^2/V sec. The output differential resistance was equal to 500 KΩ. The linearity of transconductance or gain versus input voltage V_G is shown in Figure 6. The ratio of the slope of the straight line portions in Figure 5 and Figure 6 should ideally give 2 and the experimental data yield 1.7. On the test stand (probe measurements of voltage-current output characteristics) an electron transmissivity as high as 0.9, corresponding to $\beta = 10$ and $g_m = 5$ mA/V, has been measured. During mounting on the headers and lead attachment by alloying, consistent degradation of the electron transmissivities were experienced. It was found, that the contact to the thin-film structure introduced stresses which damaged the heterojunction diode.

The planar structure was adopted, therefore, which brings the contacts out over the SiO_2 layers. During lead attachment no pressure has to be exerted on the thin-film structure.

CdS-Si SCLC-TRIODE (N-19)



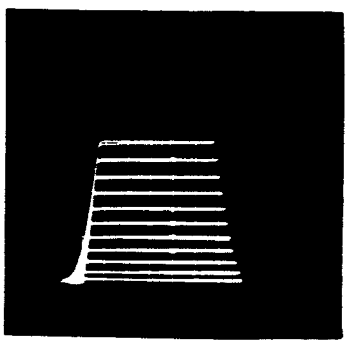
GROUNDED SOURCE V_D I_D - CHARACTERISTIC

g_{max} = 2 mA/V

V_D horizontal 2V/DIV.

I_D vertical 1mA/DIV.

+ 1V/STEP GATE VOLTAGE



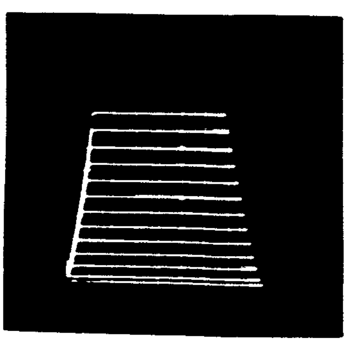
GROUNDED SOURCE V_D I_D - CHARACTERISTIC

β = 4

V_D horizontal 2V/DIV.

I_D vertical 2mA/DIV.

+ .5 mA/STEP GATE CURRENT



GROUNDED GATE V_D I_D - CHARACTERISTIC

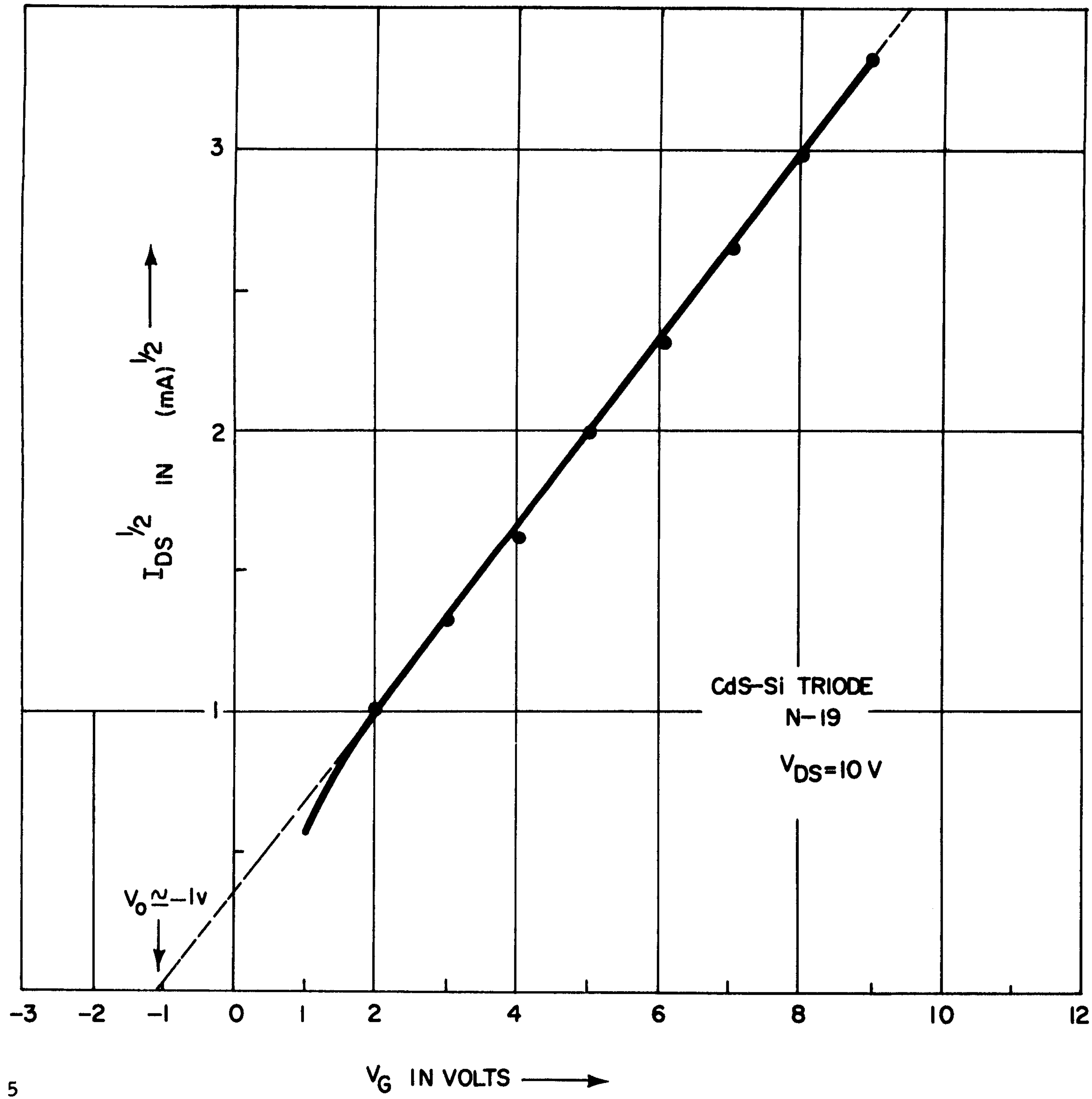
α = .8

V_D horizontal 2V/DIV.

I_D vertical 1 mA/DIV.

- 1mA/STEP SOURCE CURRENT

FIGURE 14 - Voltage-Current Output Characteristics of a CdS - Si Space-Charge-Limited Triode (N-19) in Grounded Source and Gate Configuration.



<u>FIGURE 15</u> - $I_{DS}^{1/2}$ vs. V_G of Triode N-19 at Constant V_{DS} = 10 V.

Figure 5

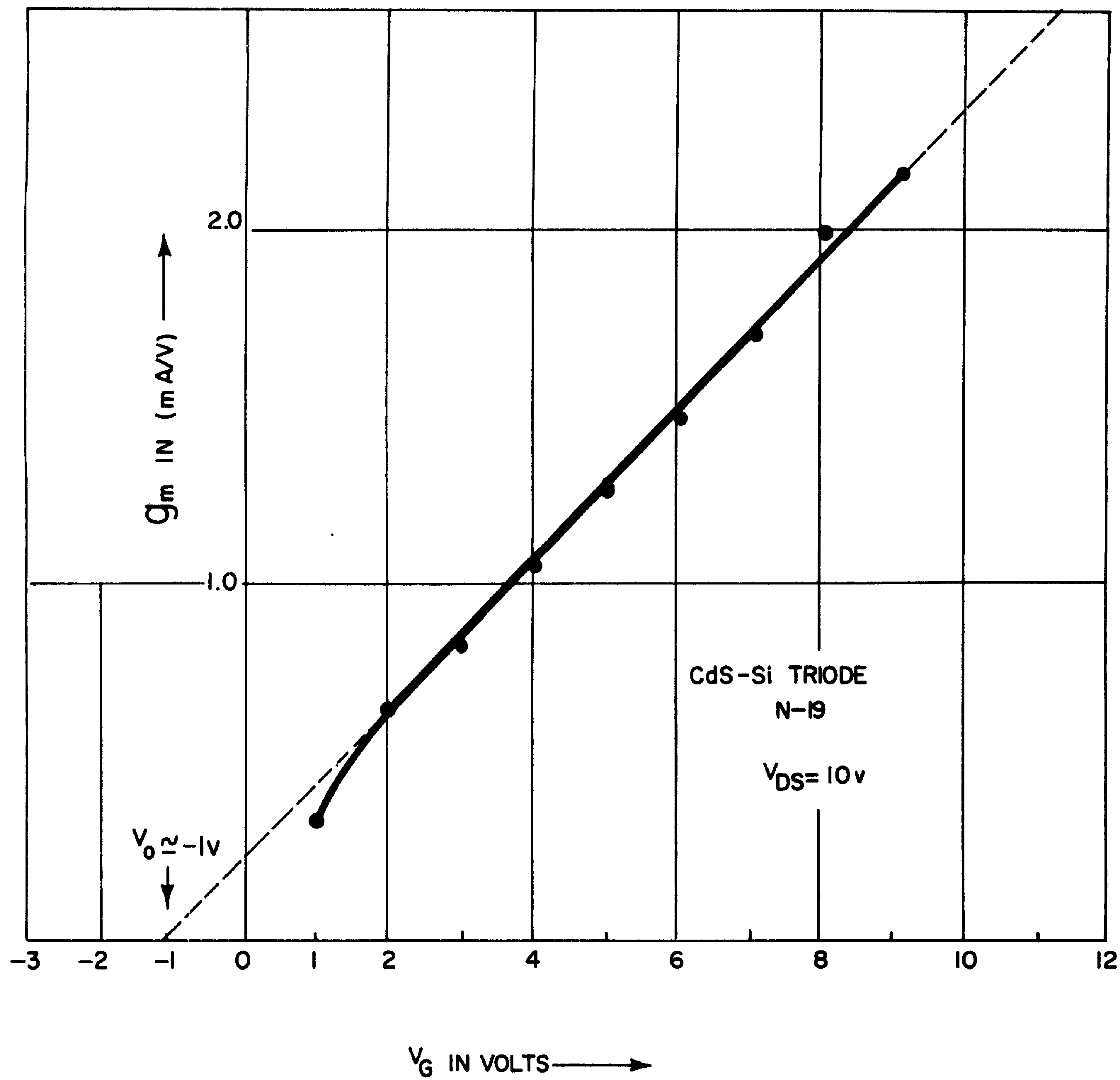


FIGURE 16 - g_m vs. V_G of Triode N-19 at Constant V_{DS}= 10V.

Figure 6

2) GaAs-Si Heterojunction Transistor

a) GaAs-Si Heterojunction Diode Evaluation:

The GaAs-Si heterojunction diode to P-type silicon was studied in detail. This diode structure is essentially the one employed for the heterojunction transistor, which should operate under space-charge-limited current conditions of the emitter diode.

Two different modes of current flow in diodes made from GaAs films deposited at 400°C and 500°C were obtained. It was realized, that either a Schottky barrier or a space-charge-limited diode could be fabricated depending upon the electronic properties of the GaAs film and the GaAs-Si interface. Results of subsequent studies concerning the metal contact properties to the GaAs film, showed that the type of diode, e.g. Schottky or space- charge-limited, is not entirely determined by the properties of the GaAs film, but depends also on the metal contact formed with the GaAs film. The deposition temperature of the GaAs film may have a lesser influence on the different mode of current flow, but could be more important in the metal contact formation to the film itself. Figure 7 shows voltage current characteristics of identical films of GaAs but provided with two different metal contacts. One diode was made with SnAu and the other one with SnNi contacts. The shift along the voltage axis at a constant current level indicates, that the SnAu contact possesses a higher voltage drop. The established Schottky relation of the voltage-current characteristic arises from the barrier, ϕ, at the GaAs-Si interface (see Figure 10). Depending upon this barrier height, the voltage current characteristic is composed of two distinct regions. As a consequence, current at small forward voltages is controlled by thermal diffusion over this barrier and for $V \gg kT/q$ this is described by

$$J = J_o \exp \left[- \frac{q(\phi - V)}{kT} \right] \quad . \qquad (9)$$

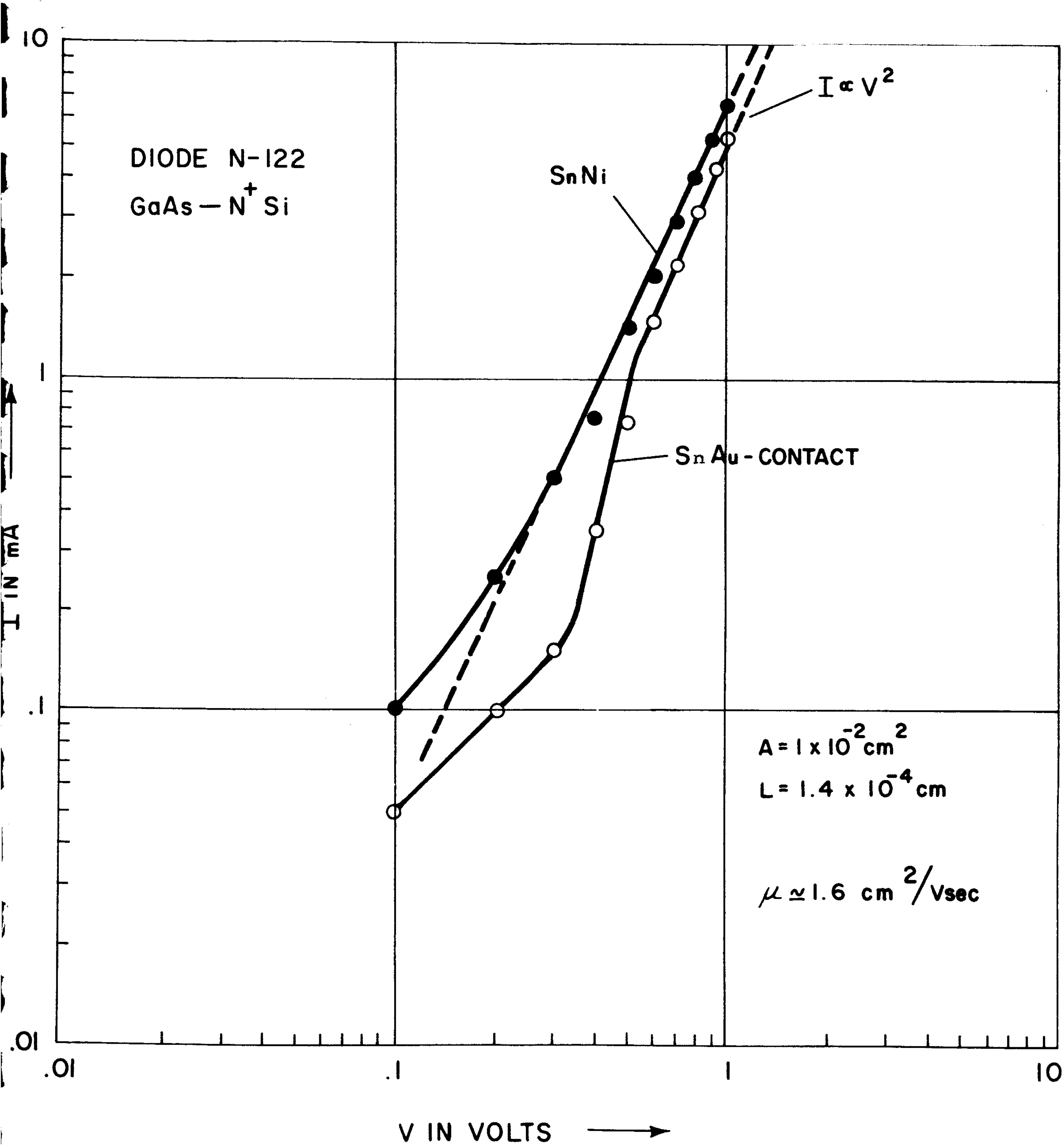

10
1
.1
.01
.01
.1
1
10
I IN mA
V IN VOLTS
DIODE N-122
GaAs — N+ Si
SnNi
I ∝ V2
SnAu - CONTACT
A = 1 x 10-2 cm2
L = 1.4 x 10-4 cm
μ ≃ 1.6 cm2/Vsec

Figure 7

where

$$J_o = 4\pi \ m^* qk^2 T^2 / \hbar^3 \tag{10}$$

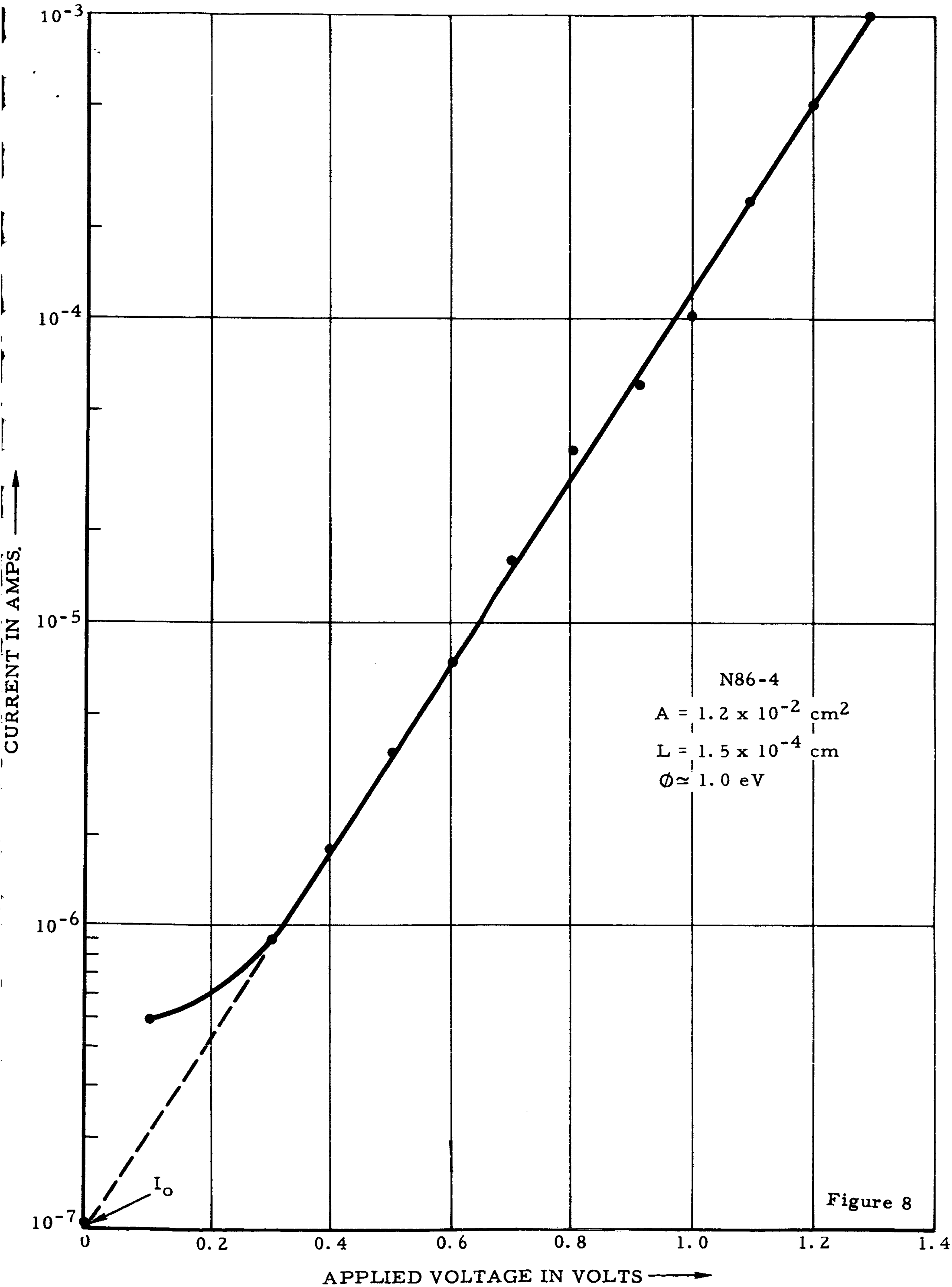
and indicates that the current should increase exponentially with voltage. This exponential relation is shown in Figure 8 in the low voltage region. The extrapolated intercept of this straight line upon the ordinate occurs at a current value corresponding to V = 0 in Equation 9 and provides a measure for ϕ. Values of ϕ obtained in this way range from 0.5 to 2.5 eV. The method is not very accurate, but the result agrees in general with values of ϕ determined by other methods, which will be given in the following section.

At larger applied voltages, greater than the potential step ϕ, the Schottky barrier is gradually lowered and the current becomes space-charge-limited. It follows the square law relation of Mott-Gurney:

$$J = \frac{9 \varepsilon \varepsilon_o \ \mu (V - V_o)^2}{8 L^3} \tag{11}$$

In this expression V_o is a threshold voltage, which is a function of ϕ and is also related to the trap density in the material. See Figure 9 for the reverse and forward current voltage characteristic. A tentative band structure model of the thin-film GaAs-Si heterojunction is shown in Figure 10. The existing barrier height, ϕ, at the GaAs-Si interface has to be surmounted by electrons before entering the P-type silicon as injected minority carriers. If the film is of sufficiently high resistivity, the electron current will eventually predominate at increasingly higher applied voltages between the metal and P^+ silicon contact, so that space-charge-limited current will commence, i.e. limited by the capacitance of the metal-semi-insulator-semicondcutor sandwich. In order to improve the space-charge-limited current operation of the structure under discussion it is therefore necessary to

a) Lower the barrier at the GaAs-Si interface
b) Improve the GaAs film properties, e.g. higher mobility



CURRENT IN AMPS.
APPLIED VOLTAGE IN VOLTS
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
N86-4
A = 1.2 x 10^{-2} cm^2
L = 1.5 x 10^{-4} cm
Ø≃ 1.0 eV
I_o

Figure 8

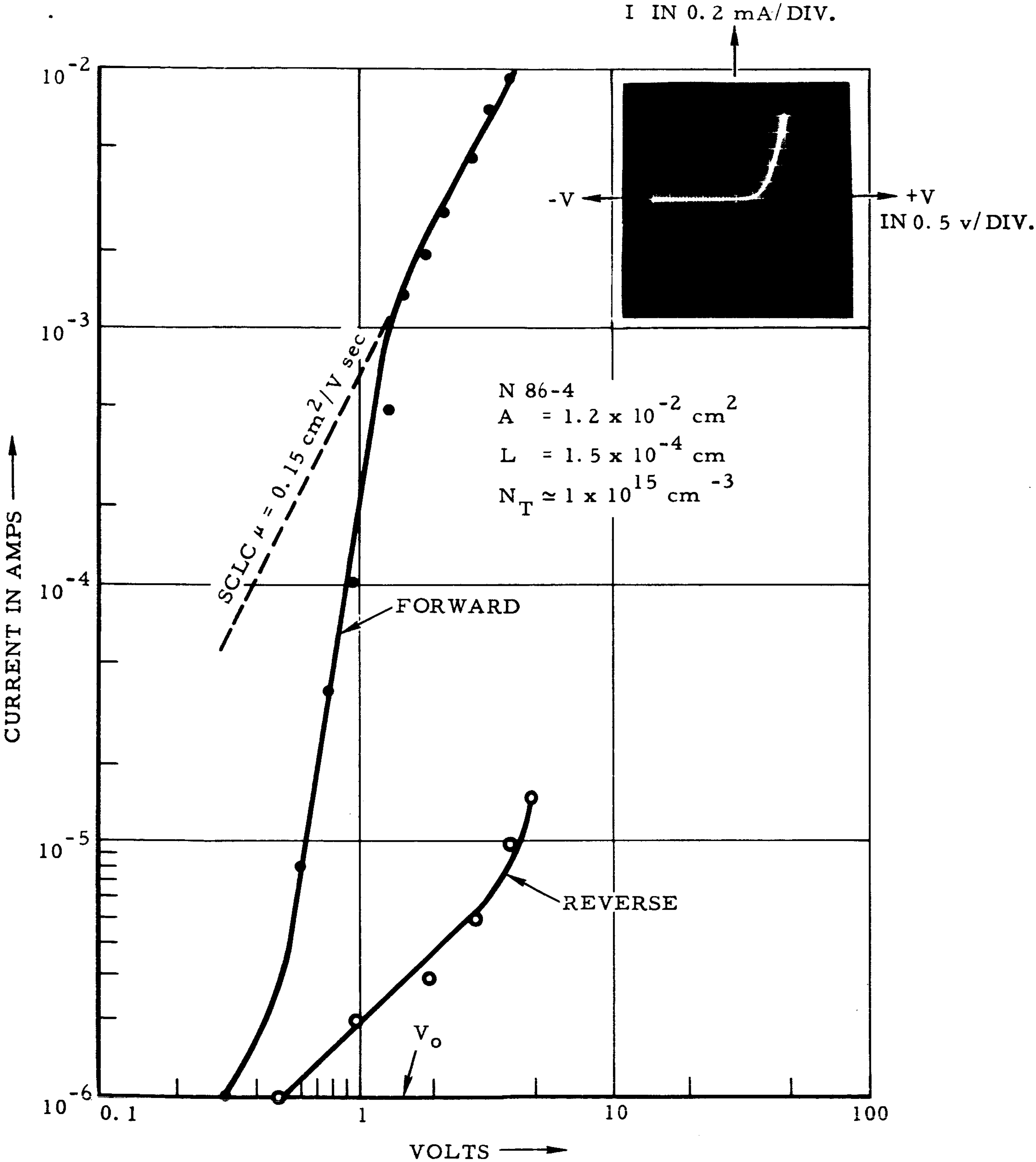
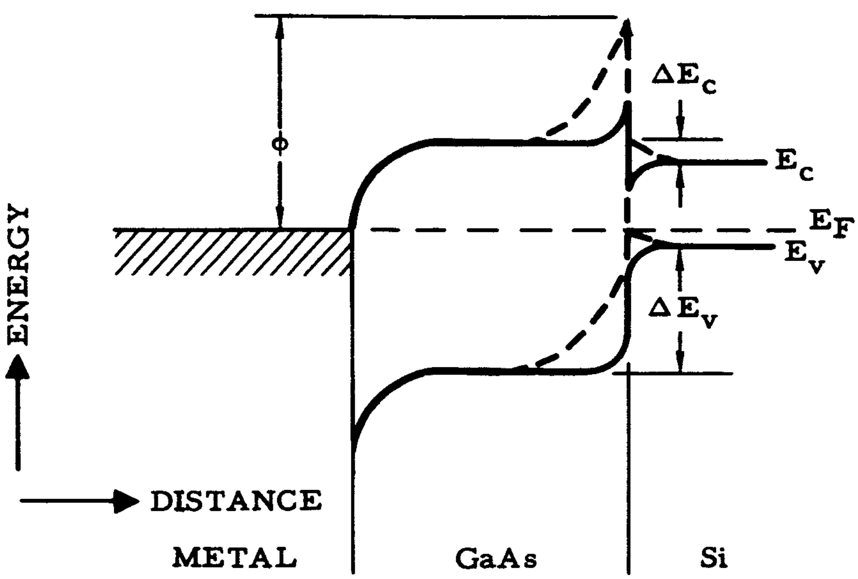

I IN 0.2 mA/DIV.
-V
+V
IN 0.5 v/DIV.
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
CURRENT IN AMPS
SCLC $\mu = 0.15\ cm^2/V\ sec$
N 86-4
$A = 1.2 \times 10^{-2}\ cm^2$
$L = 1.5 \times 10^{-4}\ cm$
$N_T \simeq 1 \times 10^{15}\ cm^{-3}$
FORWARD
REVERSE
V_o
0.1
1
10
100
VOLTS

Figure 9



ENERGY VS. DISTANCE AND BANDSTRUCTURE

Figure 10

Figure 9 gives the voltage-current characteristic of diode N84-6, typical for GaAs films deposited at 500°C. The GaAs films made at this temperature have a larger cyrstallite size and, therefore, higher mobility and possibly higher resistivity, since space-charge-limited current operation is possible. The resistivity is estimated to be $10^6\ \Omega$cm. A voltage-current measurement at room temperature of this diode is presented in Figure 9 on a log-log scale. Lampert has given the theory for space-charge-limited currents in the presence of a single trap-level and we can readily apply this theory to a model for current flow in semi-insulating GaAs films. At low voltages any injected charge is trapped and to a good approximation Ohm's law is obeyed. At high voltages space-charge due to traps is small compared with that due to injected carriers and the variation of current with voltage is given by the Mott-Gurney relation, e.g. solid-state analog of Child's law, in the form of Equation 11.

The ohmic and space-charge regions are connected by a region in which the current increases rapidly by an exponential relation of $I \propto V^m$ over a small change in voltage with m usually larger than 3. The voltage at the onset of space-charge-limited current, which was defined by Lampert as the "trap-filled-limit voltage", is just the change in potential produced by the space-charge of the filled traps, that is

$$V_o = V_{TFL} = \frac{q\,N_T\,L^2}{2\varepsilon\,\varepsilon_o}$$

From Figure 9 we obtain $V_{TFL} = 1.5$ V and with $L = 1.5 \times 10^{-4}$cm the trap density can be calculated from the above equation and is equal to

$$N_T \simeq 1 \times 10^{15}\ \text{cm}^{-3}$$

Using the slope of the space-charge-limited current relation above V_{TFL} and Equation 11 yields an effective electron drift mobility of

$$\mu_e \simeq 0.15\ \text{cm}^2/\text{V sec.}$$

This rather low value of mobility is not too surprising if we consider the polycrystalline structure of the film with small crystallite sizes. From temperature measurements of space-charge-limited current above V_{TFL} at a fixed voltage the temperature behavior of the mobility can be obtained. These measurements on diodes and prepared Hall samples indicated a mobility increase with increasing temperature according to an exponential relation

$$\mu(T) = \mu_o \exp \left[- \frac{E}{kT} \right]$$

where E is an activation energy assigned to the "hopping" process for electrons in the polycrystalline film. A lower bound for the resistivity of the films can be estimated from the mobility value and the argument that the free charges, N_D, should be less than the trapped charge density. Therefore

$$\rho \geq \frac{1}{q N_T \mu_e}$$

which gives $\rho \geq 2 \times 10^4 \, \Omega\text{cm}$.
The semi-insulating properties of the GaAs films can probably be ascribed to a deep acceptor level which compensates a shallow donor level of original and residual impurity. It is known from single crystal GaAs, that under the condition in which oxygen is present during the presentation high-resistivity and insulating material is obtained. Since during vapor deposition of the films at 10^{-6} torr still enough oxygen is present in the vacuum chamber to react with the GaAs during deposition, this compensation mechanism is most likely to occur.

The presence of the barrier height has been ascertained by two other methods, namely by the incremental capacitance measurement and photoelectric measurements.

The behavior of an ideal dielectric diode has been discussed by Shao and Wright(10). According to theory, the reverse bias incremental capacitance is equal to the geometrical electrode capacitance

$$C_o = \frac{\varepsilon \varepsilon_o A}{L} \qquad (12)$$

and the forward bias incremental capacitance is equal to

$$C_F = \frac{3}{4} C_o \tag{13}$$

The presence of the Schottky barrier results in a large incremental capacitance, because the applied voltage is developed across the barrier rather than across the full thickness of the GaAs film. A representative measurement is shown in Figure 11. At high reverse voltage the measured capacitance approaches the geometrical capacitance. Also at high forward bias, when space-charge-limited current operation is attained, the measured capacitance approaches the three-quarter value of the geometrical capacitance. The incremental capacitance of a contact area A is given by the well known Schottky relation

$$C = \left[\frac{q \varepsilon \varepsilon_o \, N_D \, A^2}{2\,(V + V_B)} \right]^{1/2} \tag{14}$$

A plot applied voltage, V, versus $1/C^2$ is shown in Figure 12. The linear relation observed around the zero bias region between applied voltages and the inverse square of the capacitance confirms that the Schottky barrier exists as described in Figure 10. The density of the ionized donors, N_D, can be obtained from the slope of this graph and is given by

$$N_D = \frac{2}{q \varepsilon \varepsilon_o \, A^2} \left(\frac{\Delta V}{\Delta \; 1/C^2} \right) \simeq 2 \times 10^{15} \; cm^{-3} \tag{15}$$

The extrapolated intercept of the straight line, $1/C^2$ versus V, on the abscissa measures V_B, the built-in potential rise through the Schottky barrier under the condition of thermal equilibrium. The measurement indicates V_B = 2.4 eV.

Photo-electric measurements were performed at the Hughes Research Laboratory (Malibu) according to a method which was successfully applied to measure the

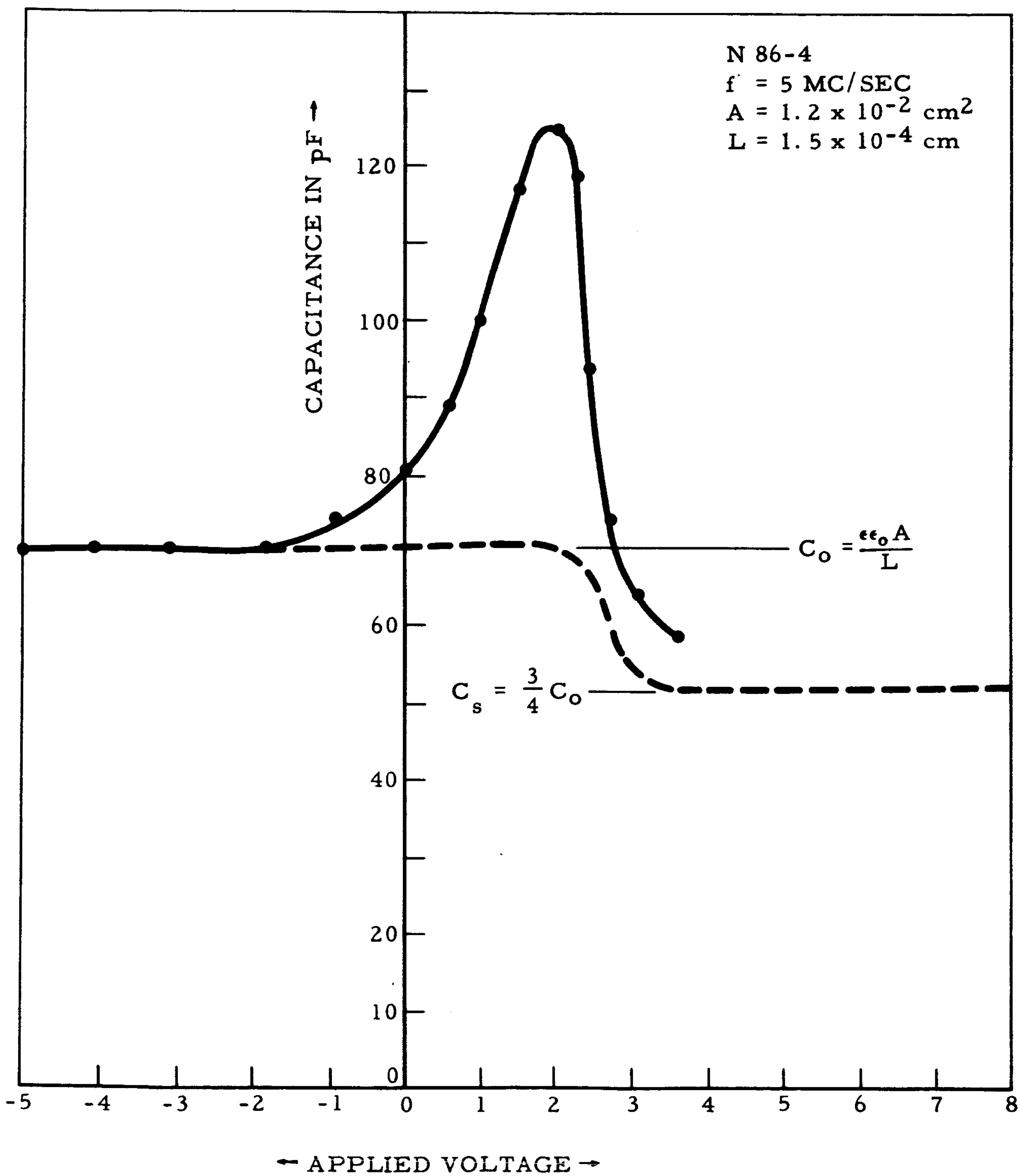
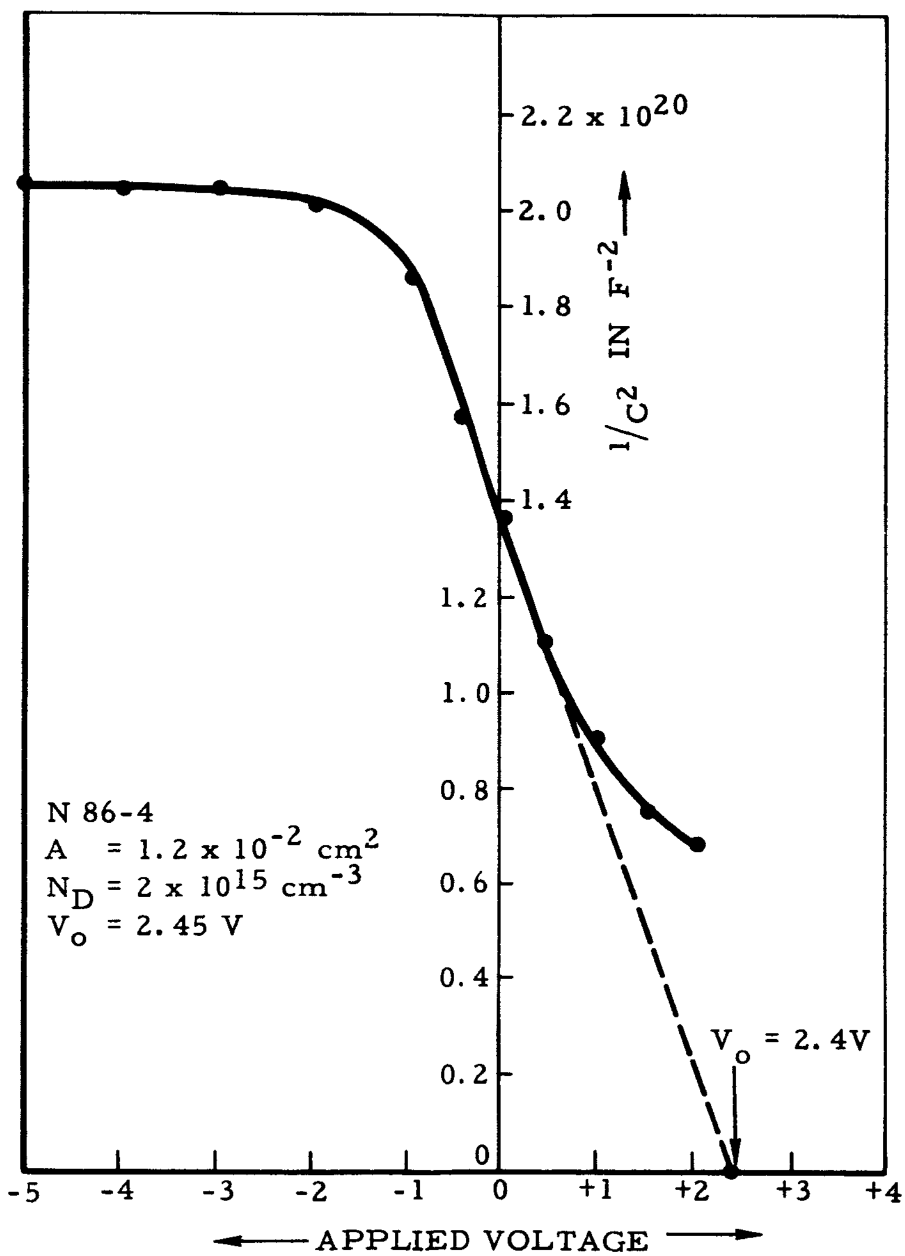

N 86-4
f = 5 MC/SEC
A = 1.2 x 10^{-2} cm^2
L = 1.5 x 10^{-4} cm
CAPACITANCE IN pF
120
100
80
60
40
20
10
0
$C_o = \frac{\epsilon\epsilon_o A}{L}$
$C_s = \frac{3}{4} C_o$
-5
-4
-3
-2
-1
0
1
2
3
4
5
6
7
8
APPLIED VOLTAGE

Figure 11



2.2 x 10^20
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0
1/C^2 IN F^-2
N 86-4
A = 1.2 x 10^-2 cm^2
N_D = 2 x 10^15 cm^-3
V_o = 2.45 V
V_o = 2.4V
-5
-4
-3
-2
-1
0
+1
+2
+3
+4
APPLIED VOLTAGE

Figure 12

barrier height of $Al-Al_2O_3-Al$ thin-film structures[11]. This measurement gives the open circuit photo voltage as a function of photon energy and is presented in Figure 13. It clearly shows the barrier height of about 2.4 eV. The relative response indicates also the bandgap of Si at 1.1 eV and GaAs at 1.5 eV. If the barrier would not be present the response curve would drop sharply at about 1.4 eV. A typical ideal response curve was reported by Anderson[12] for a Ge-GaAs heterojunction, which shows a broad maximum between about .83 and 1.4 eV. The decrease to low values in the high energy region occured at a value of 1.55 eV instead of the expected value of the GaAs bandgap (1.36 eV). The deviation of the relative photoresponse of the thin-film GaAs-Si heterojunction from the ideal curve, is therefore attributed to the formed barrier between the GaAs and Si. This barrier height determination is in good agreement with the built-in potential measurement and correlates well with the barrier height estimated from d-c measurements using Equation 9.

Negative resistance characteristics have been observed with diodes made on N-type silicon material. This negative resistance characteristic was not light sensitive and was observed also by Nizushima et al[13] on very high resistivity GaAs films. The same investigators[14] analyzed the breakdown and concluded, that field ionization is the origin of this phenomenon. With improved GaAs films, a negative resistance is frequently observed on GaAs diodes made on P^+ material. It is believed, that this is a true double injection, since

a) it is very light sensitive

b) heterojunction transistors with this kind of emitter diode have no current amplification until the current jumps to the higher current values.

A typical voltage-current characteristic of such a diode is shown in Figure 14 with and without illumination from a focused microscope lamp. Since the voltage-current characteristic after the appearance of the negative resistance shifts, modulation of the bulk conductivity is present. A heterojunction transistor with such an emitter diode, has usually very low gain up to the onset of the negative resistance region and with sufficient alpha, e.g. greater than 0.5, breaks into oscillation. This oscillation extinguishes, when the base current is increased and normal transistor action takes place. The negative or double injection characteristic can be explained as follows: Assuming a Schottky barrier at the GaAs-Si interface, with the metal contact at a negative potential, electrons

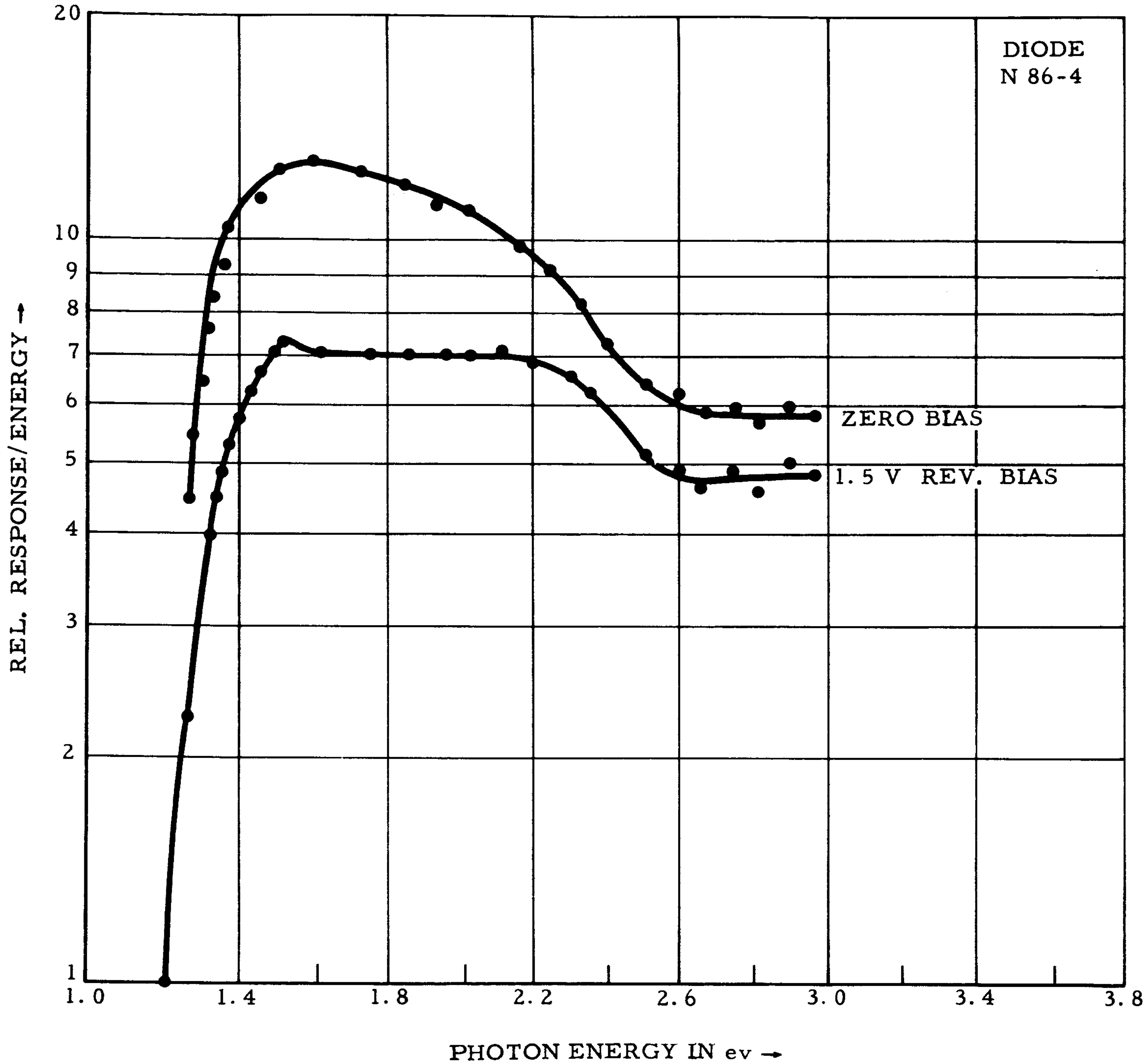

DIODE
N 86-4
ZERO BIAS
1.5 V REV. BIAS
REL. RESPONSE/ENERGY →
PHOTON ENERGY IN ev →
20
10
9
8
7
6
5
4
3
2
1
1.0
1.4
1.8
2.2
2.6
3.0
3.4
3.8

Figure 13

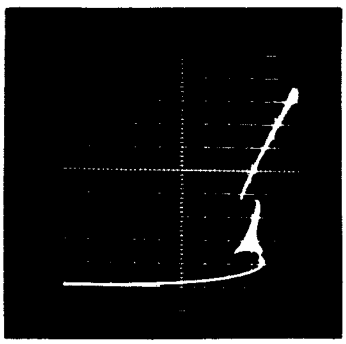
GaAs - Si HETEROJUNCTION

Diode N-150

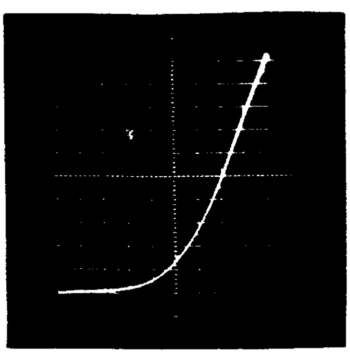
Scales:

Horizontal: Voltage in 0.5V/DIV.

Vertical: Current in 0.2mA/DIV.



No illumination



With illumination

Figure 14

are injected into the Si at reasonable voltages. However, before sufficient electron current is established in the GaAs film, the P^+ silicon contact to the other side of the GaAs film will inject holes from the large reservoir, (e.g. P-type doped silicon of 5×10^{18} cm^{-3}) of higher density than the electrons injected over the Schottky barrier. At higher voltages, electron transport will dominate, when a sufficient lowering of the barrier for electrons is encountered.

b) GaAs-Si Heterojunction Triodes:

With a diode characteristic similar to N86-4 in Figure 9 space-charge-limited triodes should become operational. Devices with the planar structure were fabricated. However, no acceptable devices with electrically good heterojunctions could be obtained at first. Investigations revealed that

i) the GaAs heterojunction to nearly degenerate P^+ surfaces of silicon with a surface concentration of $10^{19} cm^{-3}$ does not give good rectification characteristics.

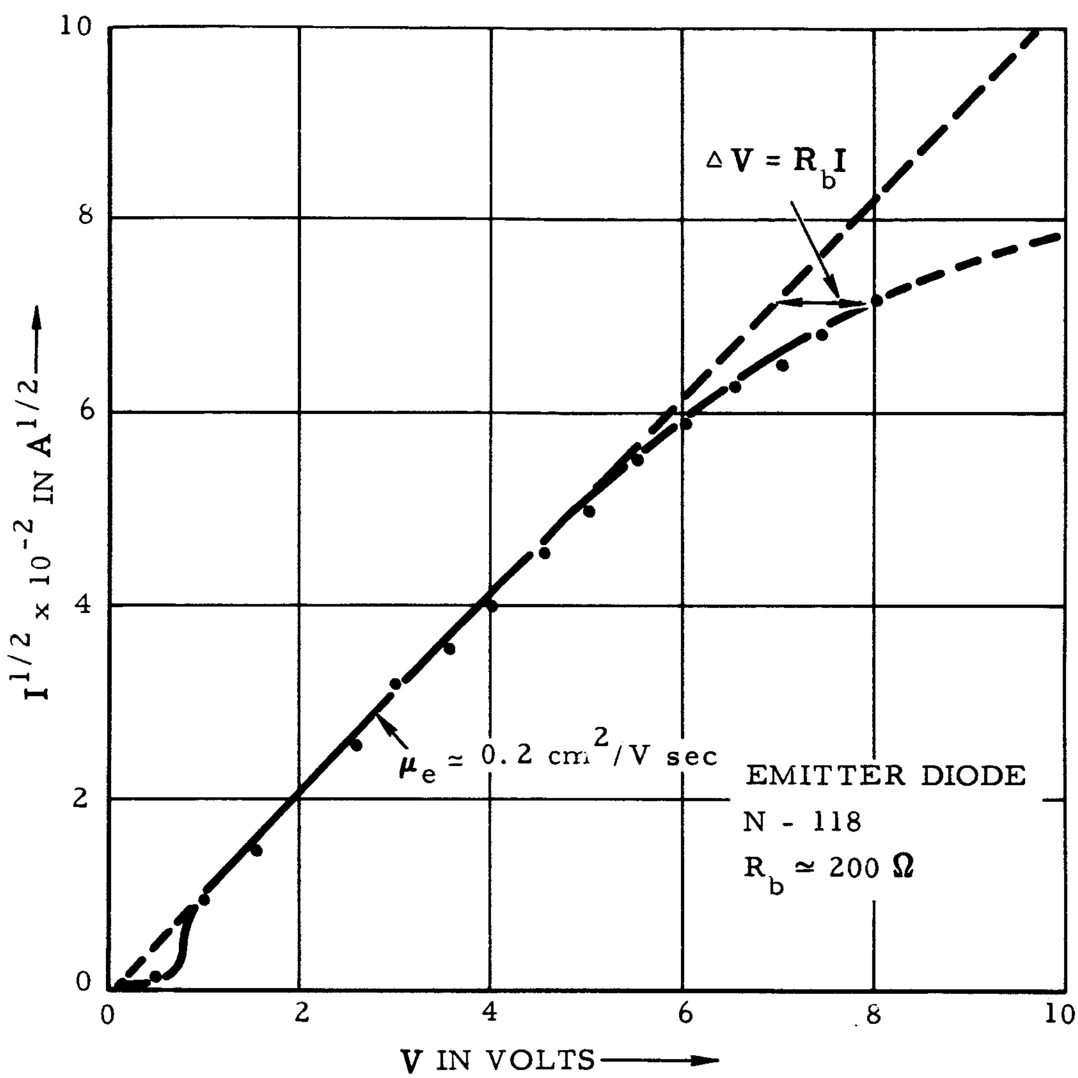
ii) during the GaAs deposition at 500°C the protected silicon PN-junction is contaminated and becomes very leaky.

The following corrective measurements were carried out

1) the surface concentration of the shallow diffused P-region was lowered to values between 1 and $5 \times 10^{18} cm^{-3}$. A more advantageous value would be around $5 \times 10^{17} cm^{-3}$, but could not be obtained so far from our diffusion group.

2) the silicon PN-junction was protected prior to GaAs deposition with a thicker layer of SiO_2, which is also terminated about 5 mils away from the junction periphery instead of the 2 - 3μ protection in the original mask design. This required a new oxide growth after the P-diffusion and additional window opening.

As a result of these changes, stable operational devices were fabricated. The GaAs-P(Si) heterojunction diode of transistor N-118 is shown in Figure 15, plotted as $I^{1/2}$ versus V. The straight line relation above 1 volt reveals the square law of space-charge-limited current. Trap-filling is completed at



10
8
6
4
2
0
0
2
4
6
8
10
$I^{1/2} \times 10^{-2}$ IN $A^{1/2}$
V IN VOLTS
$\Delta V = R_b I$
$\mu_e \simeq 0.2\ cm^2/V\ sec$
EMITTER DIODE
N - 118
$R_b \simeq 200\ \Omega$

Figure 15

about 1 volt. The deviation from the straight line above 5 volts is due to the voltage drop across the base spreading resistance. This resistance can be calculated and is in the order to 200 Ω. This value is also predicted from the geometry and the sheet resistance $R_{\square}$ of the diffused layer, which was $1880\Omega/\square$. From the geometry (see Figure 19) one can approximate

$$R_b \simeq \frac{R_{\square} S}{D} \tag{16}$$

where S is the spacing between the Al base contact and D is the diameter of the P-diffusion area. With S = 5 mils and D = 50 mils one obtains a value of 180 Ω. The transfer characteristic of the space-charge-limited emitter current to the collector, measured in saturation at constant voltage of 10 volts is shown in Figure 16. This current should be equal to

$$I_D = \alpha \frac{9\,\varepsilon\varepsilon_o\,\mu A}{8\,L^3} (V_G - V_o)^2 \tag{17}$$

From a straight line relation above two volts, in the plot of $I_D^{1/2}$ versus V_G, the square-law is revealed. Figure 17 gives the curve tracer output characteristics of triode N-118 in grounded source with voltage and current drive, Figure 17a and 17b respectively. The maximum transconductance is .4 mA/V. The maximum base current amplification factor $\beta = 3$ when considering the device as a bipolar transistor. Figure 17c then gives the grounded gate, corresponding to a grounded base operation of a bipolar transistor, and reveals an $\alpha = 0.7$.

This interfacial transmissivity, α, for the electrons through the heterojunction gate is very encouraging, when considering the possible improvements arising from a lower surface concentration e.g. $5 \times 10^{17} cm^{-3}$, which would diminish the loss of electrons by recombination in the thin P-layer and from optimized GaAs film deposition to reduce interface states. Lowering of the transmissivity is primarily due to recombination at the heterojunction interface. To demonstrate this recombination effect upon the injection efficiency and transmissivity, τ, an energy band diagram of the GaAs-Si NP-junction is shown in Figure 18. If recombination throughout the depletion regions is assumed to be negligible,

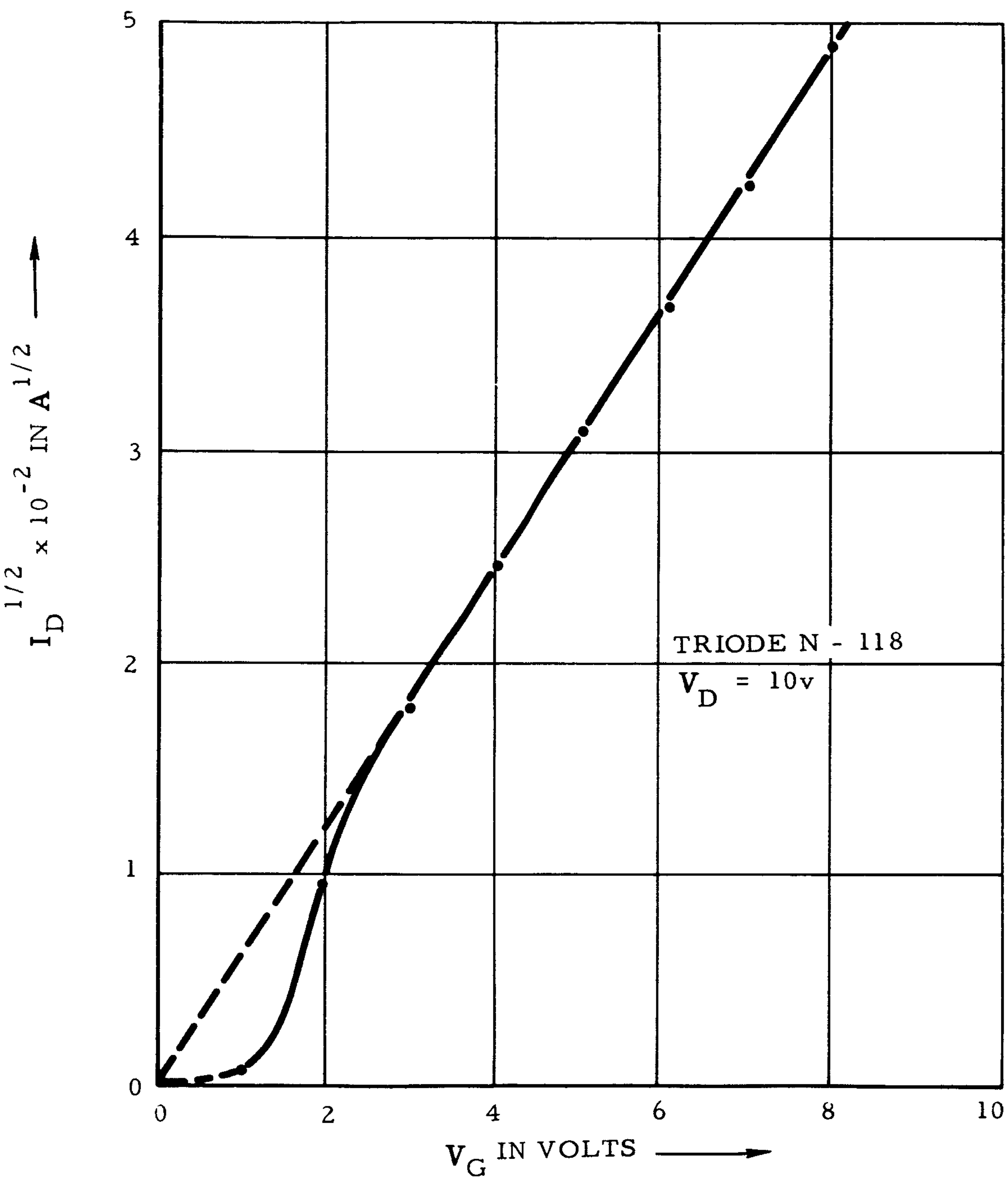
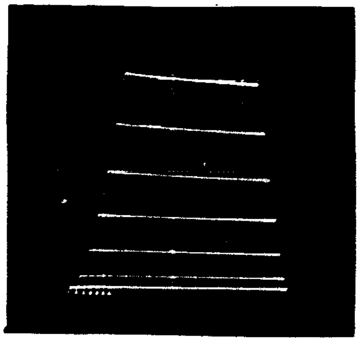

5
4
3
2
1
0
0
2
4
6
8
10
$I_D^{1/2} \times 10^{-2}$ IN $A^{1/2}$
V_G IN VOLTS
TRIODE N - 118
V_D = 10v

Figure 16

GaAs-Si SCLC-TRIODE (N-118)

A



Grounded Source $V_D I_D$-Characteristic

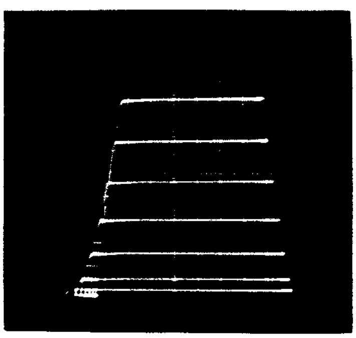
$g_{max} = .4mA/V$

V_D horizontal 2V/DIV.

I_D vertical .2mA/DIV.

+ 1V/STEP gate voltage

B



Grounded Source $V_D I_D$-Characteristic

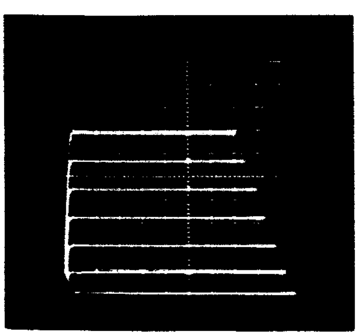
$\beta = 3$

V_D horizontal 2V/DIV.

I_D vertical .2mA/DIV.

+ .1mA/STEP gate current

C



Grounded Gate $V_D I_D$ - Characteristic

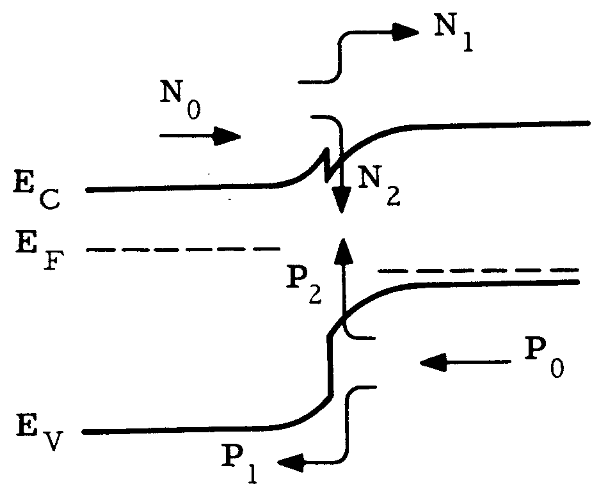
$\alpha = .7$

V_D horizontal 2V/DIV.

I_D vertical 0.5mA/DIV.

- 1 mA/STEP source current

Figure 17



A GaAs - Si NP - HETEROJUNCTION
IN FORWARD BIAS

Figure 18

then only the charges N_1 and P_1 could flow. Due to the wide gap emitter effect, i.e. the much smaller barrier height for N_1 the electron current proportional to N_1 would predominate and P_1 the hole current would tend to become zero, so that

$$\tau = \frac{N_1}{N_1 + P_1} \longrightarrow 1 \tag{18}$$

if P_1 is small.

If, however, recombination of electrons and holes takes place near the heterojunction interface in a layer of states near the center of the energy gap, then the current could consist of an additional electron current N_2 into the states from the left and a hole current P_2 into the states from the right. The transmissivity is then given by

$$\tau = \frac{N_1 - N_2}{N_1 - N_2 + P_2} \tag{19}$$

If we assume, that $N_2 = P_2$, then Equation 19 reduces to

$$\tau = 1 - \frac{N_2}{N_1} \tag{20}$$

For a triode with transmissivity approaching one, the loss current N_2 has to be reduced. For the device N-118, whose characteristics are shown in Figure 17, the loss current would amount to 30% of the total emitted current N_o. This would be true, if no additional losses would take place during the transition of charge carriers across the P-region. In general then

$$\alpha = \tau\beta \tag{21}$$

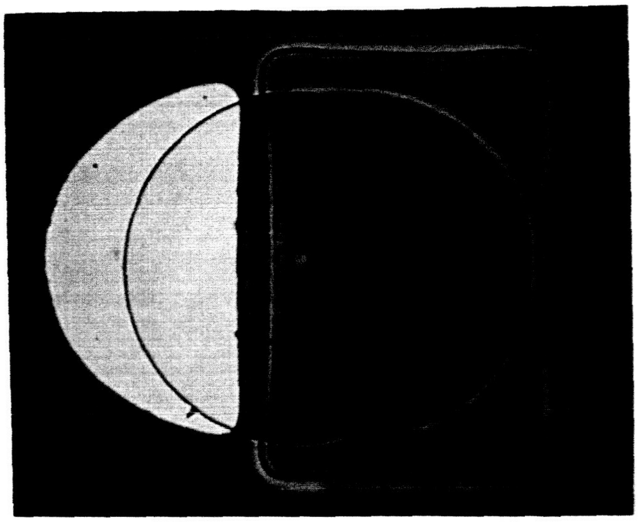
where β is the normal base transport factor. It is approximately given by

$$\beta = 1 - \frac{1}{2}\left(\frac{W}{L_n}\right)^2 \tag{22}$$

where L_n is the diffusion length for electrons, and W is the effective width of the P region.

A top view photograph of a planar thin-film space-charge-limited triode of the present design is shown in Figure 19. A cross section through this device is shown in Figure 3d. The ohmic contact to the silicon P-layer is made by an evaporated aluminum contact. The ohmic contact to the GaAs film is a tin-gold evaporated contact. Thermocompression bonding is not directly applied to the active area of both contacts. The bond is made to the portion of the contact brought out over an oxide layer. This design assures reliable and non-damaging contacts in respect to the thin-film GaAs-diode and the thin diffused P-region.

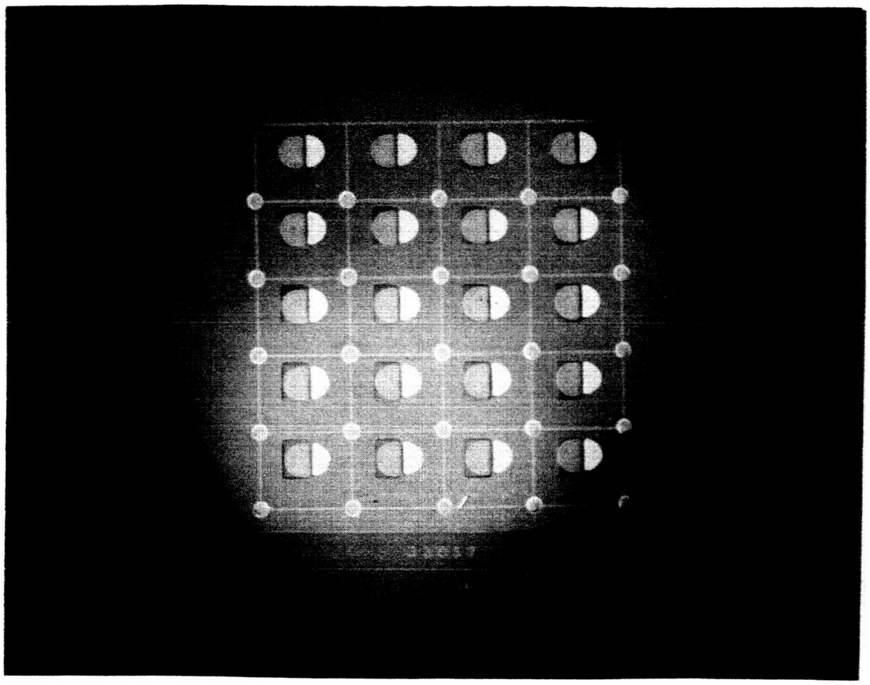
The GaAs-Si heterojunction transistor was investigated in respect to recombination losses. It was possible to fabricate with consistent yields transistors with current amplification factors between 1 and 5, when mounted on headers and transistors with beta's as high as 10 when tested by point contact probes on the original silicon wafer after completing processing. Figure 20 is a photograph of 20 GaAs-Si heterojunction transistors which are processed by employing planar silicon technology and vapor deposition of a GaAs-film to form the heterojunction of GaAs to Si. The structure is described in Figure 3. A typical grounded emitter voltage-current characteristic of devices under investigation with a beta equal to five is shown in Figure 21. In general, the devices indicate a beta versus collector current behavior similar to homojunction, bipolar transistors. At low collector currents the amplification is low due to recombination losses at the surface and interfaces. It then rises to a maximum in a current range of 2 to 10 mA and above this peak value starts to decrease probably due to crowding effects. Since the amplification factors were so consistent, investigation was made as to whether or not the impurity distribution in the silicon P-type base and the surface preparation of the silicon prior to the deposition of the GaAs-film has influence upon the amplification properties. The base width was changed from 0.5μ to about 2μ and the surface concentration varied from 5×10^{19} to $2 \times 10^{18} cm^{-3}$ with no noticeable changes in amplification properties. Perhaps the changes are small and of second order, with first order effects ascribed to recombination losses at the GaAs-Si interface. Prior to GaAs-film deposition, the silicon surface was cleaned:



Top View Photograph of a Planar Thin-Film Space-Charge-Limited Triode.

Diameter of Circle is 50 mils.

Figure 19



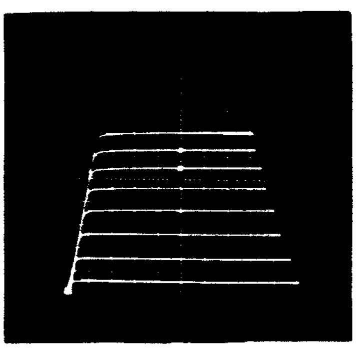
150 mils

SILICON WAFER WITH 20 GaAs-Si

PLANAR HETEROJUNCTION TRANSISTORS

Figure 20

GaAs-Si HETEROJUNCTION TRANSISTOR



GROUNDED EMITTER CHARACTERISTIC

SCALES:

Vert. Collector Current I_C in 0.5 mA/DIV.

Horiz. Collector to Emitter Voltage V_{CE} in 1 volt/DIV.

Pos. Base Current I_B in 0.1mA/STEP

$$\beta = \frac{\Delta I_C}{\Delta I_B} \simeq 5$$

Figure 21

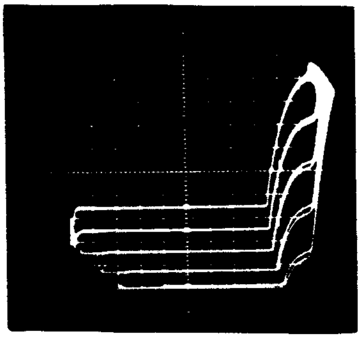
a) with hot HCl etch in an epitaxial reactor

b) by standard chemical means, e.g. CP_4

and no significant improvements could be obtained. Another investigation was carried out, which also did not result in noticeable improvements. The investigation was concerned with different silicon base materials, that is, epitaxial material compared to parent silicon material from a single crystal ingot and silicon material with and without the diffused base. The purpose of these experiments was to see if different surface conditions would result in better GaAs nucleation and consequently fewer surface states. All experiments turned out to give negative results, which indicated, that the recombination mechanism at the GaAs-Si interface is the determining factor for the electrical functioning of the heterojunction transistors. Figure 22 shows a set of grounded base and grounded emitter characteristics for a device with an alpha of about 0.6. This device was made with a base diffusion, whereby punchthrough to the emitter occurs before breakdown of the collector-to-base PN junction. The punchthrough to the emitter depletion region is 45 volts. Beyond this voltage, bipolar transistor operation is not possible, since alpha becomes unity and in grounded emitter configuration voltage saturation occurs (= breakdown). It should be noticed, that after the onset of punchthrough a considerable voltage has to be added, before the alpha becomes unity. The range of this incremental voltage indicates the amount of band bending and the presence of interface states at the GaAs-Si before the actual punchthrough to the GaAs emitter region occurs, at alpha equal to unity, at approximately 55 volts. This experimental result, when compared with behavior of homojunction transistors, establishes without doubt the deleterious effects and consequences of heterojunctions when employed for the construction of bipolar transistors. Owing to the unavoidable interfacial states in heterojunctions, band bending effects and recombination of excess minority carriers are expected. The evidence in our investigation is the consistent reduction of alpha to values of 0.5 to 0.8 and the absence of minority carriers storage effects. A typical switching characteristic of a GaAs-Si heterojunction transistor is shown in Figure 23. The transient effects are mainly determined by charge and discharge of the interface-states and override completely the charge effects in the base and in the collector region of the device, which are much shorter. The switching speed and high frequency performance of the present devices is therefore a function of the emitter time-constant. The advantages of

GaAs-Si HETEROJUNCTION TRANSISTOR

N - 147



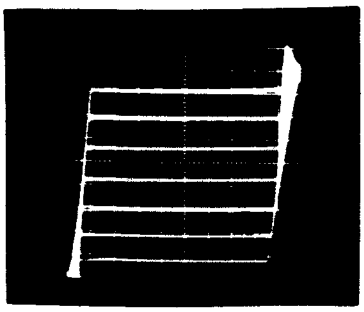
GROUNDED BASE CHARACTERISTIC

SCALES:

Vert. Collector Current in 0.5 mA/DIV.

Horiz. Collector Voltage in 5 V/DIV.

Emitter Current in 1 mA/STEP



GROUNDED EMITTER CHARACTERISTIC

SCALES:

Vert. Collector Current in 0.2 mA/DIV.

Horiz. Collector Voltage in 5 V/DIV.

Base Current in 0.1 mA/STEP

Figure 22

SWITCHING PERFORMANCE OF
GaAs-Si HETEROJUNCTION TRANSISTOR

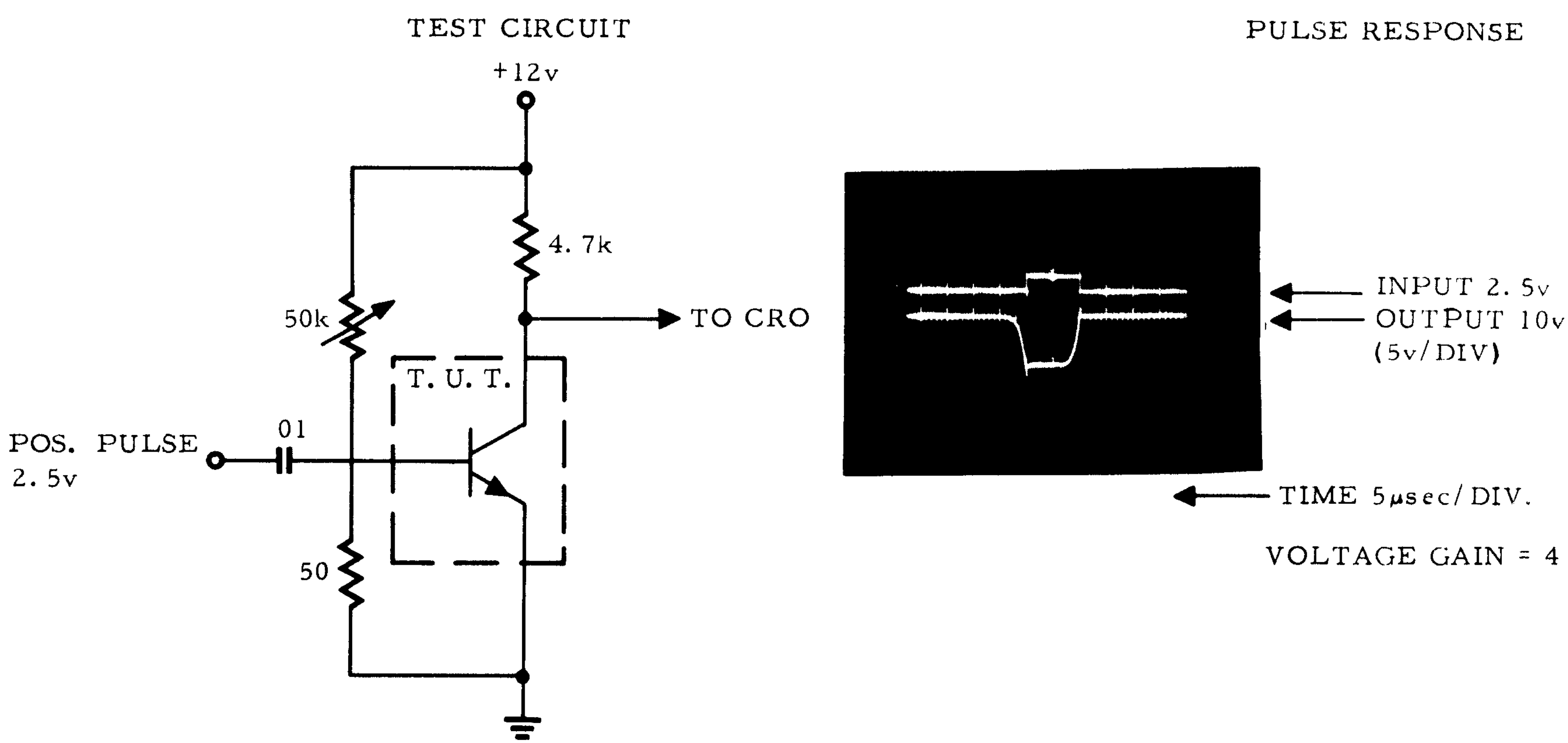


Figure 23

a high emitter cut-off device[15, 16] cannot be realized until ideal space-charge-limited emitter diode operation is achieved. Oldham and Milnes[17] have shown theoretically, that dislocations alone resulting from a mismatch of 0.05 percent in the lattice constants of the two single crystal semiconductors would lead to minority carrier transmission coefficients of 0.3 to 0.6. Since the alpha of a wide gap emitter of heterojunction transistor cannot exceed this minority carrier transmission coefficient in the absence of multiplication, it is concluded, that efficient operation of heterojunction or wide-gap emitter is very unlikely to be achieved with the variety of known semiconductors and the various preparation techniques available today. If the lattice mismatch in percent is defined by [17]

$$LM = \frac{2(\lambda_2 - \lambda_1)}{\lambda_1 + \lambda_2} \times 100 \qquad (23)$$

where $\lambda_1 < \lambda_2$ and the λ's are the respective lattice constants for the two semiconductor materials forming the heterojunction, we can compute the following values

Heterojunction	LM
Ge-GaAs	0.07%
Si-GaAs	2.00%
Ge-Si	4.00%

Since Ge-GaAs gives the best lattice match and even for this case the minority transmission coefficient was estimated to be in the range from 0.27 to 0.58[17], the Si-GaAs heterojunction should be worse. No matter what heterojunction construction is used, the lattice mismatch would produce at least 5×10^{13} cm^{-2} dangling bonds in single crystal junctions. Bardeen[18] has shown that surface state densities in the order of 10^{13} cm^{-2} or greater are sufficient to dominate metal semiconductor barrier formation. Since the densities of these interface states will largely determine the position of the Fermi level at the heterojunction interface we are confronted with two major effects, when heterojunction operation is considered:

a) bending of bands at the heterojunction, as shown by Oldham and Milnes[17]

b) recombination losses at the interface due to interface states as indicated by the absence of minority carrier storage in Si-GaAs heterojunction diodes and transistors, as verified by experiment during this contract.

The results of alpha's as high as 0.9 experimentally achieved with the GaAs-Si heterojunction transistor seem to indicate, that the interface states may not be as deleterious to the operation of heterojunctions as predicted by Oldham and Milnes[17]. This statement is supported by the fact, that the GaAs-Si heterojunctions under question are not really single crystal junctions, although the GaAs film is highly oriented in the (111) plane but of polycrystalline structure, containing therefore in addition to the dislocation states an excess amount of other defects at the interface. Theory and experiment of interfacial states, although not in very good agreement, have established the importance of the mere presence of states to the operation of heterojunctions. The ideal heterojunction band structure as shown in Figure 10 (solid lines) warrants a closer examination and the band bending could be as shown in the dashed lines. This band shaping could also be inferred from measurements on n-n and p-p heterojunctions consisting of various semiconductor materials with different lattice mismatchings and was discussed and experimentally verified by Oldham and Milnes[17] and other investigators[19, 20].

In analogy to bipolar transistors, the frequency response can be characterized by the frequency f_T, where beta has obtained a value of unity. This frequency is given by

$$f_T = \frac{1}{2\pi\,(\tau_e + \tau_b)} \tag{24}$$

where

$$\tau_e = \frac{4}{3}\left(\frac{d_e}{\mu_e V_e}\right)^2 \tag{25}$$

and

$$\tau_b = \frac{d_b^{\,2}}{\mu_b V_b} \tag{26}$$

Assuming for comparison, that $d_e = d_b$, the ratio of the transit-times is

$$\frac{\tau_e}{\tau_b} = \frac{4}{3} \cdot \left(\frac{\mu_b V_b}{\mu_e V_e}\right) \tag{27}$$

This relation indicates, that for $\mu_b \simeq \mu_e$ and since $V_e >> V_b$, a real high frequency response could be achieved with the heterojunction transistor in view of $\tau_e << \tau_b$. Only the base-transit time has to be taken into consideration. This theoretical argument for the heterojunction transistor is in contrast to the bipolar transistor frequency response, where $\tau_e > \tau_b$ and the transistor is said to operate in the emitter cut-off region. The actual heterojunction transistor however has an effective mobility μ_e, which is much smaller than μ_b, so that $\tau_e > \tau_b$ and it also operates in the emitter cut-off region. For a numerical example, we select $\mu_b = 1000 cm^2/V$ sec., $\mu_e = 1\ cm^2/V$ sec., $V_e = 2$ volts, and $V_b = 0.2$ volts, which was obtained from the relation for the built-in drift field voltage

$$V_b = \frac{kT}{q} \ln \left(\frac{N_E}{N_C}\right) \tag{28}$$

with $N_E \simeq 5 \times 10^{18} cm^{-3}$ and $N_C = 1 \times 10^{15} cm^{-3}$, so that finally

$$\frac{\tau_e}{\tau_b} \simeq 13$$

With low mobility films of GaAs or CdS, it is therefore not possible to realize the high frequency operation of the heterojunction transistor and the device operates similar to the bipolar transistor inthe emitter cut-off region. Since both types of transistors, namely the homojunction and the heterojunction bipolar, operate in the emitter cut-off region it is instructive to look at the respective emitter time constants. For the normal bipolar transistor

$$\tau_{eN} = r_e C_e = \frac{kT}{qI_e} C_{eN} \tag{29}$$

and for the heterojunction transistor operating under space-charge-limited emitter current

$$\tau_{eH} = r_e C_e = \frac{V_e}{2I_e} \quad C_{eH} \tag{30}$$

Assuming that both devices have the same emitter capacitance C_e and operate at the same current I_e, then

$$\frac{\tau_{eH}}{\tau_{eN}} = \frac{q V_e}{2k T} \tag{31}$$

which gives a factor of 40 for $V_e = 2$ volts and $kT/q = 0.025$ volts. The heterojunction transistor therefore has a lower frequency response, when only the differential resistances come into play. The advantage of the heterojunction transistor, as claimed by G. T. Wright, should be the lower capacitance, C_{eH}, due to space-charge-limited current operation. This capacitance however can only be obtained, when the GaAs or CdS film is made rather thick. Then the current is reduced proportional to d_e^{-3}, whereas the capacitance is reduced only proportional to d_e^{-1}. Therefore, to achieve the low capacitance operation at a reasonable current level and using a thicker GaAs or CdS emitter region, it is necessary to have a material of high mobility. The mobility should be at least within a factor of ten of the electron mobility in the base region of the heterojunction structure. For the device structures under investigation $C_{eH} \simeq 60$ pF (see Figure 11) and $r_e \simeq 500\Omega$, for $V_e = 2$ volts, and $I_e = 2$ mA (see Figure 9) so that

$$f_{TH} = \frac{1}{2\pi \, r_e C_e} \simeq 5 \text{ MHz}$$

The bipolar transistor for the same current level and same capacitance would have

$$f_{TN} \simeq 200 \text{ MHz}$$

c) A Method for Determination of Trapping Effects:

Theoretical Model - Fundamental properties of trapping states in thin single crystals or polycrystalline films of semiconductors or semi-inculators can be studied by means of their frequency-sensitive behavior obtained from admittance or impedance measurements. Muller[21, 22] has analyzed the behavior for CdS thin single crystals containing traps for the case of one injecting and one ohmic, and two injecting contacts, and predicted a theoretical admittance variation with frequency in insulators having traps subjected to charge injection.

For trapping centers more than a few kT above the steady-state Fermi level, the rate equation for the trapped-charge density N_T is given by the difference between the rates of filling and emptying, and can be written in the form[23]

$$\frac{dN_T}{dt} = - (N_T - \gamma N)\, \omega_e \qquad (32)$$

where N_T is the trapped-charge density, N is the free-charge density, ω_e is the probability-of-escape frequency for a trapping center and γ is the equilibrium ratio between trapped and free charges.

For the case of thermal equilibrium and shallow trapping levels

$$\omega_e = N_c \; v \; S_T \; \exp \; - \left[\frac{W_c - W_T}{kT} \right] \qquad (33)$$

where N_c is the effective density of conduction band states, v is the electron thermal velocity (10^7 cm/sec at 300°K), S_T is the capture cross section of an empty trap for a conduction-band electron and $(W_c - W_T)$ is the trap-depth below the conduction-band.

For a sinusoidal voltage excitation, $V = V_o \cos \omega t$, the time dependence of N will depend on the nature of contacts applied to the structure. If we have one injecting or ohmic contact and assume proportionality between applied voltage and injected charge density, then the waveform for the conduction band density, during excitation will be a half-wave rectified sinusoid with a peak value of N_m. Using a Fourier analysis of the wave-form we can write

$$N = \frac{1}{2} N_m \cos \omega t \tag{34}$$

which inserted into Equation 32 yields the rate equation

$$\frac{d N_T}{d t} = - \left[N_T + \frac{1}{2} \gamma N_m \cos \omega t \right] \omega_e \tag{35}$$

This linear differential equation can be solved by assuming a solution of the form

$$N_T(t) = A \sin \omega t + B \cos \omega t \tag{36}$$

which results for the steadystate term in

$$N_T(t) = \frac{1}{2} \gamma N_m \quad \frac{\cos \omega t}{1 + \left(\frac{\omega}{\omega_e}\right)^2} + \frac{\omega \sin \omega t}{\omega_e \left[1 + \frac{\omega}{\omega_e}\right]^2} \tag{37}$$

In phase with the applied voltage is the first term in parenthesis of Equation 37 and represents the trapped charge capacitance variation with frequency. If the maximum capacitance at very low frequency is C_{oT}, then the capacitance variation with frequency is given by

$$C_T(\omega) = \frac{C_{oT}}{1 + \left(\frac{\omega}{\omega_e}\right)^2} \tag{38}$$

Since the second term in Equation 37 is 90° out of phase with the applied voltage and has a derivative in phase with it, it represents a current in phase with the voltage. The term is equivalent to a conductance assigned to the conduction mechanism between traps and the conduction band. The equivalent parallel conductance, $G(\omega)$ as a function of frequency is then given by

$$\frac{G(\omega)}{\omega} = \frac{\omega \; C_{oT}}{\omega_e \left[1 + \frac{\omega}{\omega_e}\right]^2} \tag{39}$$

$G(\omega)/\omega$ goes through a maximum where $\omega = \omega_e$, which gives the value of ω_e. From the value of $G(\omega)/\omega$ at the maximum, which is equal to $C_{oT}/2$, one can calculate C_{oT}.

A theoretical plot for $C_T(\omega)$ and $G(\omega)/\omega$ is given in Figure 24.

An equivalent network can be constructed which represents the analog to trap-filling. The charge Q_c, stored in the capacitor, is analogous to the density of filled traps N_T, provided that ω_e^{-1} is taken to be proportional to the time constant RC and V_s is taken to be proportional to γN. This network is shown in Figure 25. A parallel capacitance of, C_D, was added which represents the depletion layer capacitance in the absence of any trapping. Noting that

$\omega_e = (R_T C_{oT})^{-1}$, the network admittance is

$$Y = \frac{\omega^2 C_{oT}}{\omega_e \left[1 + \left(\frac{\omega}{\omega_e}\right)^2\right]} + j\omega \left(C_D + \frac{C_{oT}}{1 + \left(\frac{\omega}{\omega_e}\right)^2}\right) \tag{40}$$

where the real part is a conductance equivalent to that in Equation 39 and the imaginary part represents a susceptance of a capacitance equal to Equation 38. Equation 40 therefore is the analog to the steady state solution of Equation 37.

Application to Semi-insulating GaAs Films - Thin-film GaAs heterojunction diodes fabricated on NN^+ and PP^+ silicon substrates were subjected to alternating current measurements and transient response measurements. Since the high resistivity GaAs film of preferentially oriented polycrystalline structure contains certainly a sizeable number of traps, the following experimental results are valuable information:

i) in application of these diodes to a three-terminal active device
ii) in respect to electrical properties of the GaAs films fabricated with the "three-temperature-method".

The GaAs-PP^+ (Silicon) diode N86-10 has been evaluated by the method outlined in the previous section. The parallel equivalent capacitance and the resistance

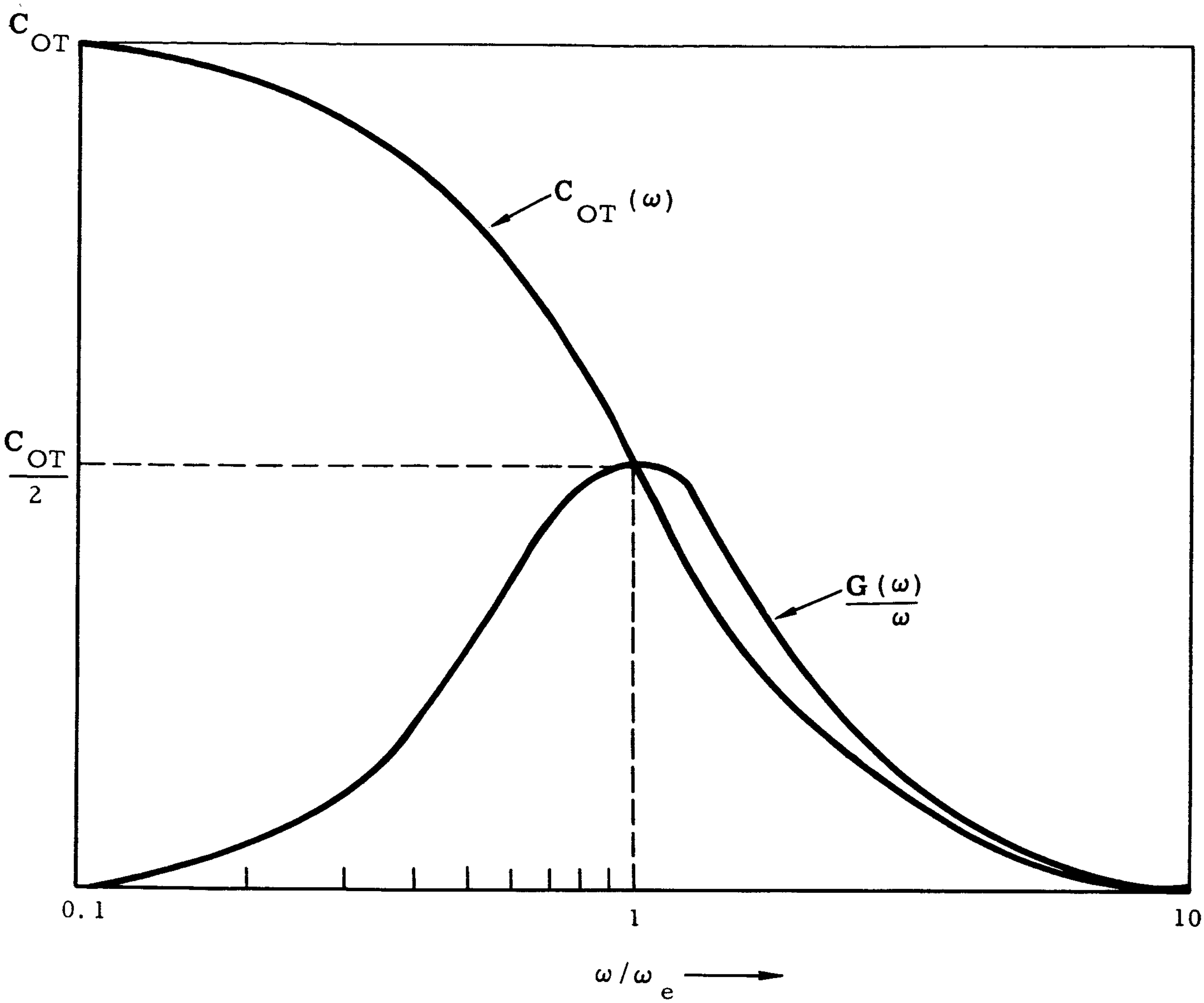
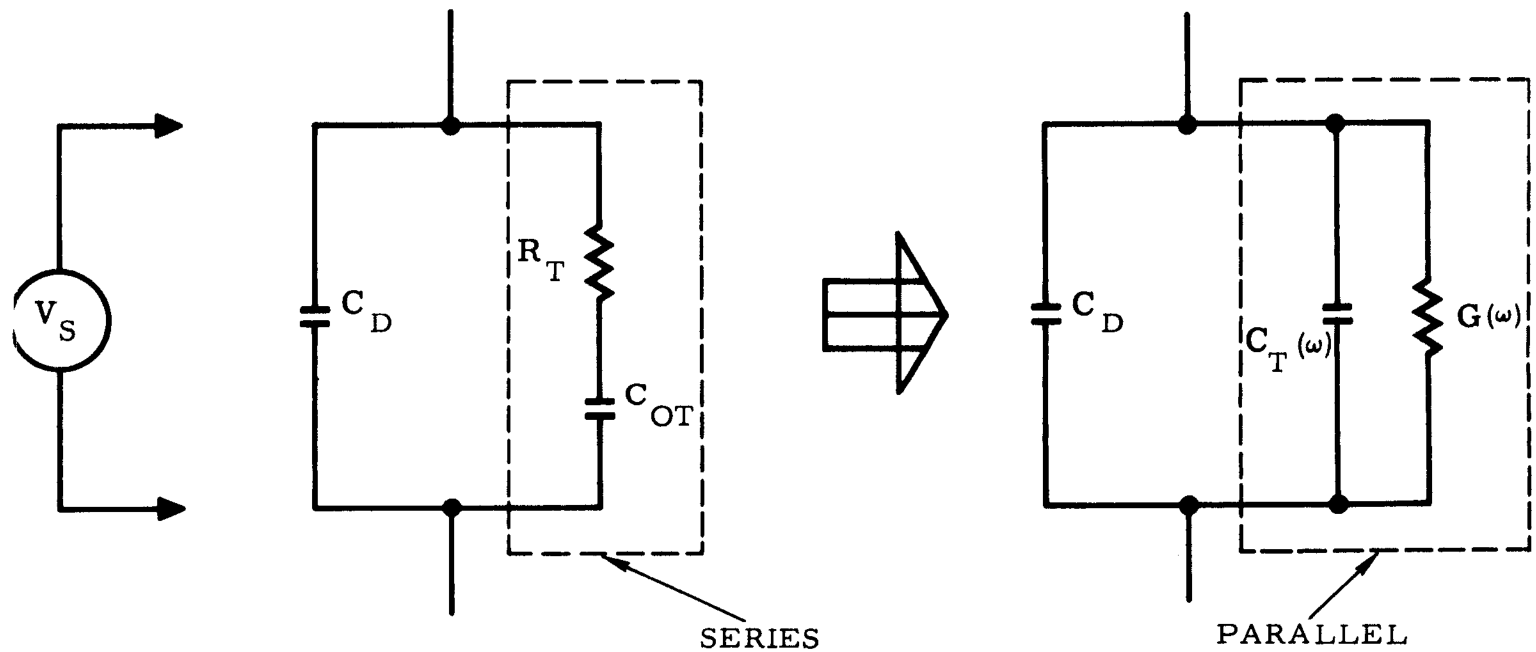

C_{OT}
$C_{OT}(\omega)$
$\frac{C_{OT}}{2}$
$\frac{G(\omega)}{\omega}$
0.1
1
10
ω/ω_e

Figure 24



EQUIVALENT NETWORK
TO TRAP MODEL

Figure 25

was measured on a Wayne-Kerr B-601 radio frequency bridge. The parallel equivalent resistance was converted into the conductance, and the values of $C(\omega)$ and $G(\omega)/\omega$ are presented in Figure 26 in a frequency range from 1 KG/sec to 10 MC/sec. These experimental data conform generally with the ideal curves of Figure 24. The deviation of $G(\omega)/\omega$ measured function from the ideal solution indicates probably the super-position of very slow traps, e.g. surface states at the heterojunction interface with the faster volume distributed traps. To determine surface state parameters by the technique described here, Nicollian and Goetzberger[24], and Lehovec[25] have recently published measurements on the SiO_2-Si interface.

The following information can be extracted from the experimental results of Figure 26:

The angular probability-of-escape frequency

$$\omega_e = 2\pi f_e \tag{41}$$

can be obtained at the maximum of $G(\omega)/\omega$ or at $C_{oT}/2$ and yields 30 KC/sec. Insertion of the condition $\omega = \omega_e$ into Equation 39 yields

$$\frac{G_{max}(\omega)}{\omega_e} = \frac{C_{oT}}{2} \tag{42}$$

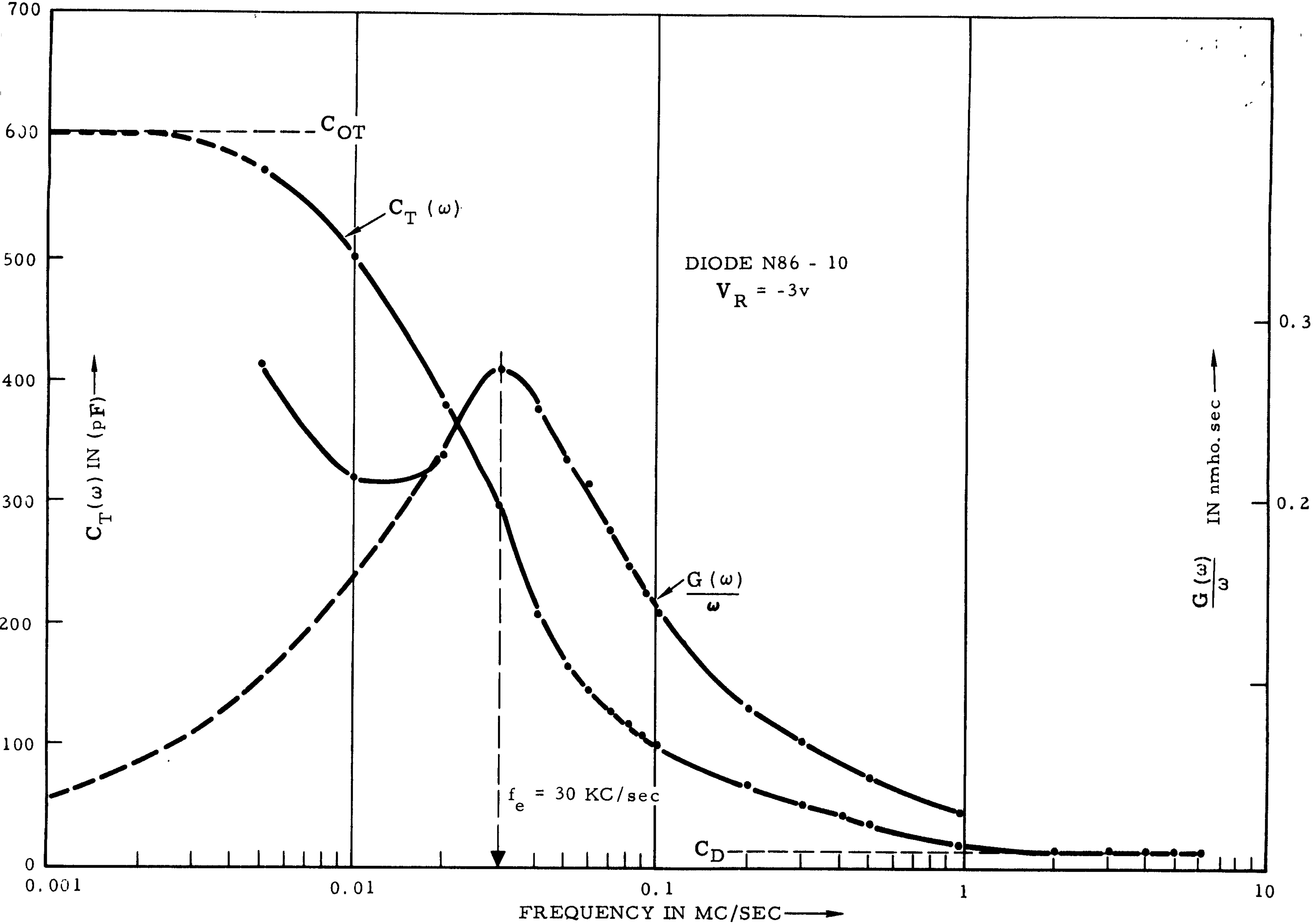
From the measured value $G_{max}(\omega)/\omega_e = .28 \times 10^{-9}$ mho sec and $f_e = 30$KC/sec one obtains from Equation 42 a value of

$$C_{oT} \simeq 570 \text{ pF}$$

which is in close agreement with the extrapolation of the $C_T(\omega)$ function to the very low frequency ranges when ω approaches zero. Above a frequency of about 1 MC/sec the capacitance is frequency independent and yields the depletion layer capacitance, C_D, equal to 20 pF.

Since the probability-of-escape frequency is (see Equation 33)

$$\omega_e = v\, S_T\, N_c \exp\left[-\frac{W_c - W_T}{kT}\right]$$



700
600
500
400
300
200
100
0
$C_T(\omega)$ IN (pF)
C_{OT}
$C_T(\omega)$
DIODE N86 - 10
V_R = -3v
0.3
0.2
$\frac{G(\omega)}{\omega}$ IN nmho. sec
$\frac{G(\omega)}{\omega}$
f_e = 30 KC/sec
C_D
0.001
0.01
0.1
1
10
FREQUENCY IN MC/SEC

Figure 26

one can calculate the capture cross section, S_T, when the location of the trap level below the conduction band is known. This value can be approximately ascertained from conductivity measurements which are performed at a low voltage applied in the forward or reverse bias condition of the diode. In this region ohmic relations are exhibited. The conductivity of diode N85-10, as a function of the inverse absolute temperature is shown in Figure 27 and yields

$$W_c - W_T \simeq 0.28 \text{ eV}$$

The number of charges in the conduction band for GaAs, at a temperature of 300°K is

$$N_c = 2\,(2\pi \; m_e \; kT/\hbar^2)^{3/2} \simeq 1 \times 10^{18} \text{cm}^{-3} \tag{43}$$

With $\omega_e = 2\pi$ (30 KC/sec), $v = 10^7$cm/sec, $N_c = 1 \times 10^{18}\text{cm}^{-3}$, and $W_c - W_T = .28$ eV we obtained a capture cross section for electrons of

$$S_T \simeq 2 \times 10^{-15}\text{cm}^2$$

The trap density may be estimated with the aid of the assumption that the Fermi level, W_F, is located at W_T, so that for the Maxwell-Boltzman statistic the trap density is given by

$$N_T = N_c \; \exp \left[- \frac{W_c - W_T}{kT} \right] \tag{44}$$

and yields a value of $N_T \simeq 2 \times 10^{13}\text{cm}^{-3}$. It should be noted that this trap density is only assigned to the deepest level. The total number of traps could be much larger, if other and more shallow levels are present. This seems to be the case as indicated by a second peak in $G(\omega)/\omega$ at a lower frequency. (see Figure 26)

Transient response measurements were made on several diodes when switching from a steady state forward current injection of about 5 mA to a reverse bias of 5 volts observing the transient recovery characteristic. Figure 28 gives the recovery characteristic of diode N86-10 and a normal PN-junction alloy silicon diode of the same junction area. The silicon diode recovery in Figure 28a is

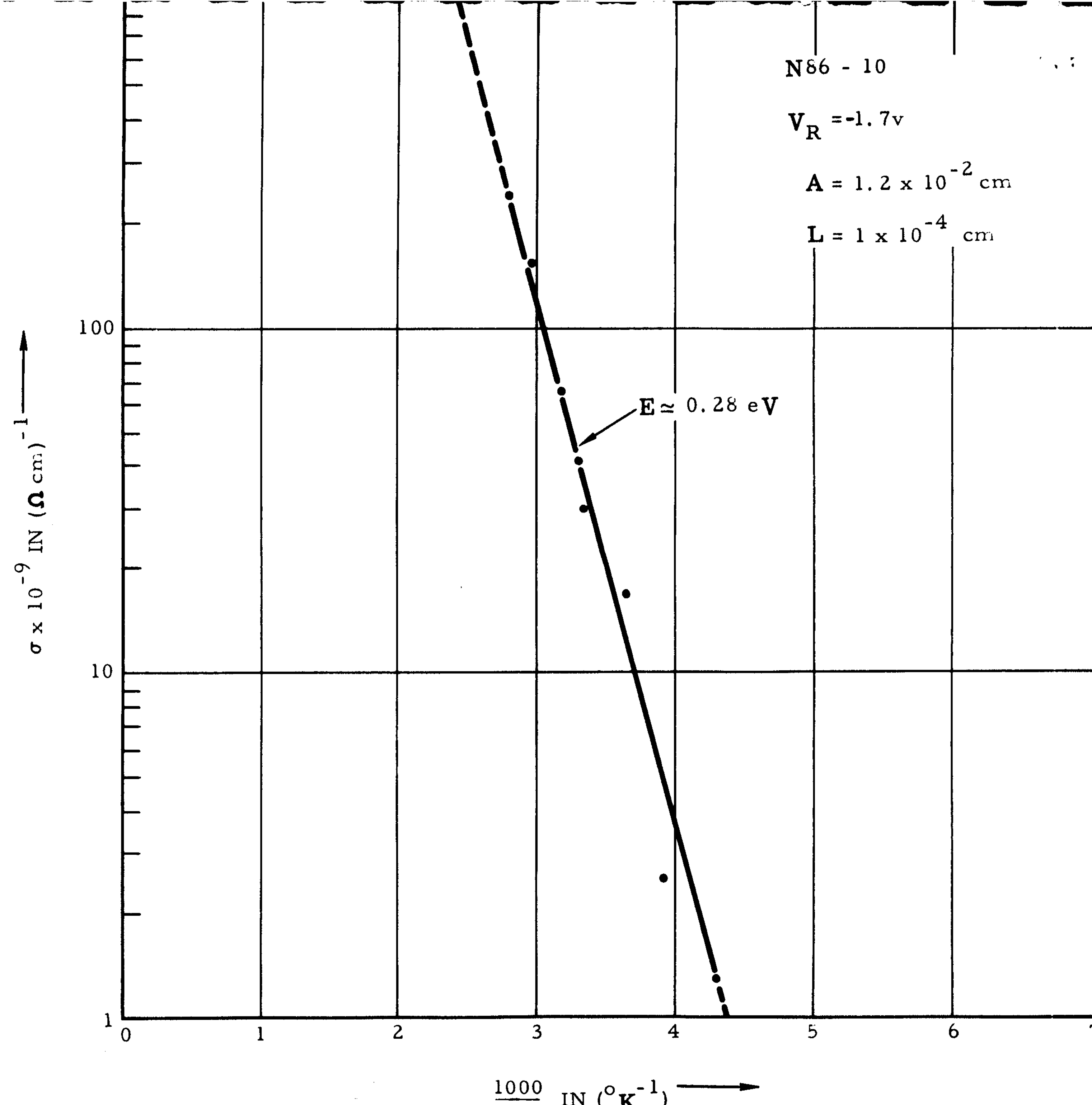
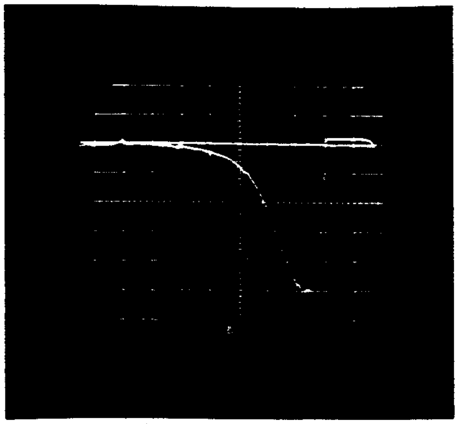

N86 - 10
V_R =-1.7v
A = 1.2 x 10^{-2} cm
L = 1 x 10^{-4} cm
E ≃ 0.28 eV
100
10
1
0
1
2
3
4
5
6
7
σ x 10^{-9} IN (Ω cm)$^{-1}$
$\frac{1000}{T}$ IN (°K^{-1})

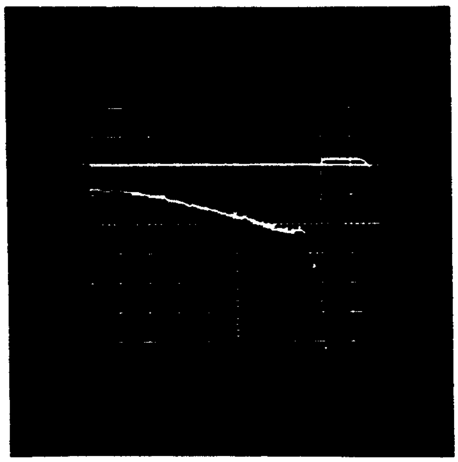
Figure 27



(a)

PN-Junction Silicon Diode.

Time Scale from right to left
in 5n sec/DIVISION.



(b)

GaAs-Si Heterojunction Diode

Time scale from right to left
in 5 n sec/DIVISION

Figure 28

the expected transient when injected minority carriers are present and swept out. With a loop impedance of 100Ω and a zero bias capacitance of 100 pF, a time constant of $\tau = 10^{-8}$ sec was expected for this diode, which corresponds roughly to the 1/e decay of the actual recovery. The recovery of N86-10 is shown in Figure 28b. Two transients are obvious. A very short one with a time constant of about 2.5×10^{-9} sec, which corresponds to the majority carrier transient of the "intrinsic" heterojunction without trapping effects. The calculated capacitance is 25 pF which should be compared to the measured C_D = 20 pF at high frequency, e.g. above 1 MC/sec. The indicated fast recovery should be expected from a true heterojunction. Deterioration of the frequency response with a long time constant is due to the trapping effects. When suddenly the reverse polarity is applied to the diode which was operated under forward bias in the space-charge-limited mode then the fast transient corresponds to charges removed from the N^+ ohmic contact to the GaAs-film and the P^+ silicon, e.g. equivalent to the charges on the plates of a capacitor. However, the filled traps will release also their charges with a lesser speed and cause the additional recovery current. If we express the external current by an exponential decay of time constant t_o, then

$$I_{ex}(t) = I_{ex}(o) \exp \left[- \frac{t}{t_o} \right] \tag{45}$$

which can be set equal to

$$I_{ex}(t) = \int q N_T A \frac{dx}{dt} \tag{46}$$

Upon equating and integrating from t = 0 to t = ∞ and x = 0 to x = L, one obtains the total number of traps emptied, which is equal to

$$N_T = (-) \frac{I_{ex}(o)\, t_o}{q\, AL} \tag{47}$$

Inserting the measured values of $I_{ex}(o) \simeq 5$ mA, $t_o \simeq 30 \times 10^{-9}$ sec, $A = 1.2 \times 10^{-2} cm^2$ and $L = 1 \times 10^{-4}$ cm yields

$$N_T \simeq 8 \times 10^{14} cm^{-3}$$

This value should be compared to the value of $N_T = 1 \times 10^{15} cm^{-3}$, which was determined from the traps-filled-limit voltage, V_{TFL}, (see Figure 9). The ionized donor concentration, which is assumed to be close to the trap density, was determined from differential capacitance versus voltage measurements (see Figure 12) and gave a value of $N_D \approx N_T \approx 2 \times 10^{15} cm^{-3}$. The value for the trap density of $N_T \approx 2 \times 10^{13} cm^{-3}$ as determined from the relation in Equation 44, should be assigned only to those traps located at 0.28 eV below the conduction band. The more realistic values of total trap density of $8 \times 10^{14} cm^{-3}$ and $1 \times 10^{15} cm^{-3}$ must be considered as a summation over all traps N_{Ti} at a location W_{Ti} according to

$$N_T = \sum_i N_{Ti} = N_c \sum_i \exp \left(- \frac{W_c - W_{Ti}}{kT} \right) \tag{48}$$

3) Discussion and Conclusion

Vapor deposited heterojunctions of either high resistivity CdS or GaAs to Si are capable of operating under space-charge-limited current conditions. Using the CdS-Si heterojunction as an electron emitter, heterojunction transistors with an alpha of 0.9 were fabricated. Under prolonged forward or reverse bias, the diodes showed changes in electrical characteristics. The GaAs-Si heterojunctions were found to be superior in respect to stability. The higher inherent mobility of GaAs over CdS was, however, not obtained with the vapor deposited films. The GaAs-Si heterojunction transistors were fabricated in a planar structure and alpha's in the range from 0.8 to 0.9 were obtained. Frequency measurements indicated, that the frequency response is primarily limited by the emitter cut-off, similar to that of a normal bipolar transistor. Only with improved electron mobility of the CdS or GaAs film one could expect the high frequency operation of such a device due to a low and current independent emitter capacitance arising from space-charge-limited operation. Trapping effects and interface states cause serious storage phenomena and reduce the switching speed. The lattice mismatch of the two semiconductor materials to form the heterojunction generate states, which lead to recombination losses and thus determine the electron transfer efficiency. This recombination phenomenon causes a base current flow, so that minority and majority carrier transport is involved, similar to the normal bipolar transistor action.

SECTION C

THE THIN-FILM SPACE-CHARGE-LIMITED TRIODE WITH DIELECTRIC SURFACE GATE STRUCTURE

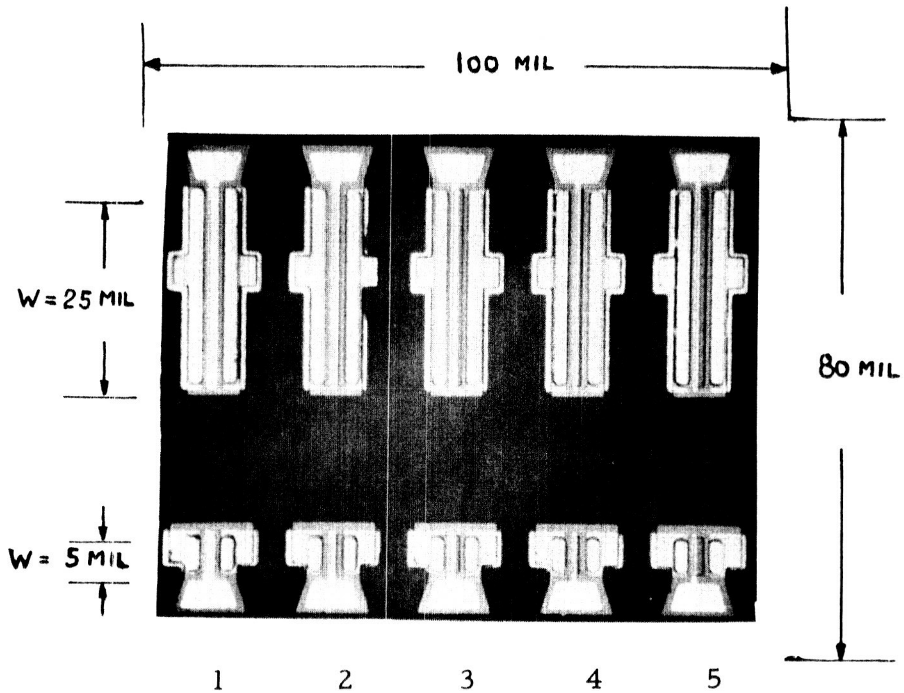
C) THE THIN-FILM SPACE-CHARGE-LIMITED TRIODE WITH DIELECTRIC SURFACE GATE STRUCTURE

1) Design, Theory and Experiment

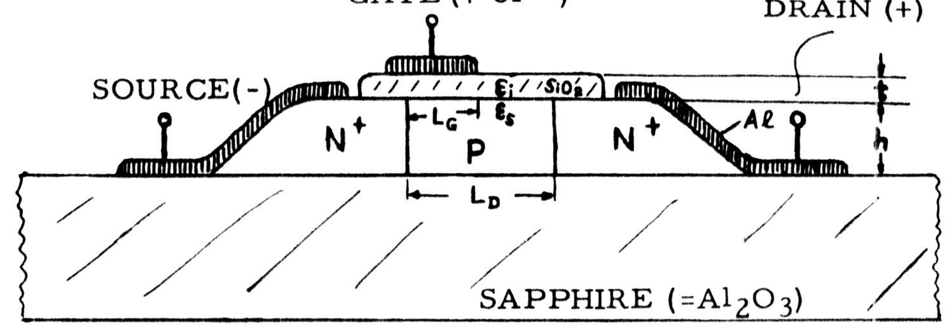
This thin-film space-charge-limited triode employs the dielectric surface gate structure and is fabricated with silicon-on-sapphire technology. It was fabricated and electrically evaluated in its basic structure under this contract. Figure 29 shows a photograph of a sapphire chip containing ten thin-film devices with varying geometries. Device No. 4 with $L_D = 10\mu$ and $L_G = 5\mu$, was found to be the best high frequency geometry for the thin-film space-charge-limited triode fabricated with this mask design and present material properties. This is by no means the optimum design of a thin-film space-charge-limited triode and with improved structures a frequency response of several GHz can be expected. The space-charge-limited triode structure is shown in Figure 29 which defines the geometrical and material parameters to be used in the theoretical evaluation and discussion. Two PN^+-junctions and one insulated gate electrode are essential to the device. The source PN^+-junction is forward biased and the drain PN^+-junction is reverse biased. The condition is obtained by grounding the source and applying a positive bias on the drain. If the bias is made sufficient enough that the depletion region for the junction of the drain extends all the way across to the source, than a normal "punchthrough" condition is established. The band diagram for this condition is shown in Figure 30a. In the P-region the current flow is by electrons and is space-charge-limited because of the high resistivity of the depleted region and the finite transit-time. The modulation of the current is by the gate electrode. A negative bias depresses the potential distribution around the source PN^+-junction, thus decreasing the drain current. Drain current is very small until the drain junction punches through to the source junction. This current is essentially the reverse saturation of a PN^+-junction. The substrate doping and the distance between drain and source determine the magnitude of the voltage at which punch-through occurs, which is given by

$$V_P = \frac{q N_A L_D^2}{2 \varepsilon_s \varepsilon_o}$$

PHOTOGRAPH OF SAPPHIRE SUBSTRATE WITH 10 THIN-FILM MOS-TRANSISTORS



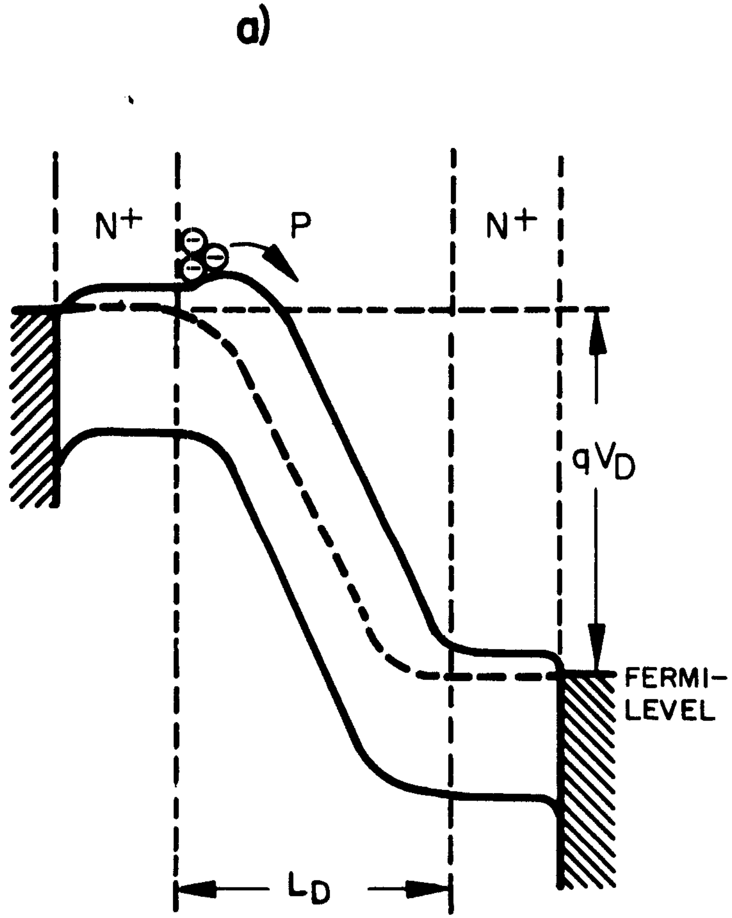
Device 1	$L_D = 20\mu$	$L_G = 20\mu$	(Pentode)
2	$L_D = 10\mu$	$L_G = 10\mu$	(Pentode)
3	$L_D = 20\mu$	$L_G = 10\mu$	(Triode)
4	$L_D = 10\mu$	$L_G = 5\mu$	(Triode)
5	$L_D = 20\mu$	$L_G = 5\mu$	(Triode)



CROSS SECTION OF THIN-FILM SPACE-CHARGE-LIMITED TRIODE

Figure 29

FIELD-LINE MAPS OF SCL-TRIODE OPERATION



BAND-STRUCTURE OF SCL- TRIODE

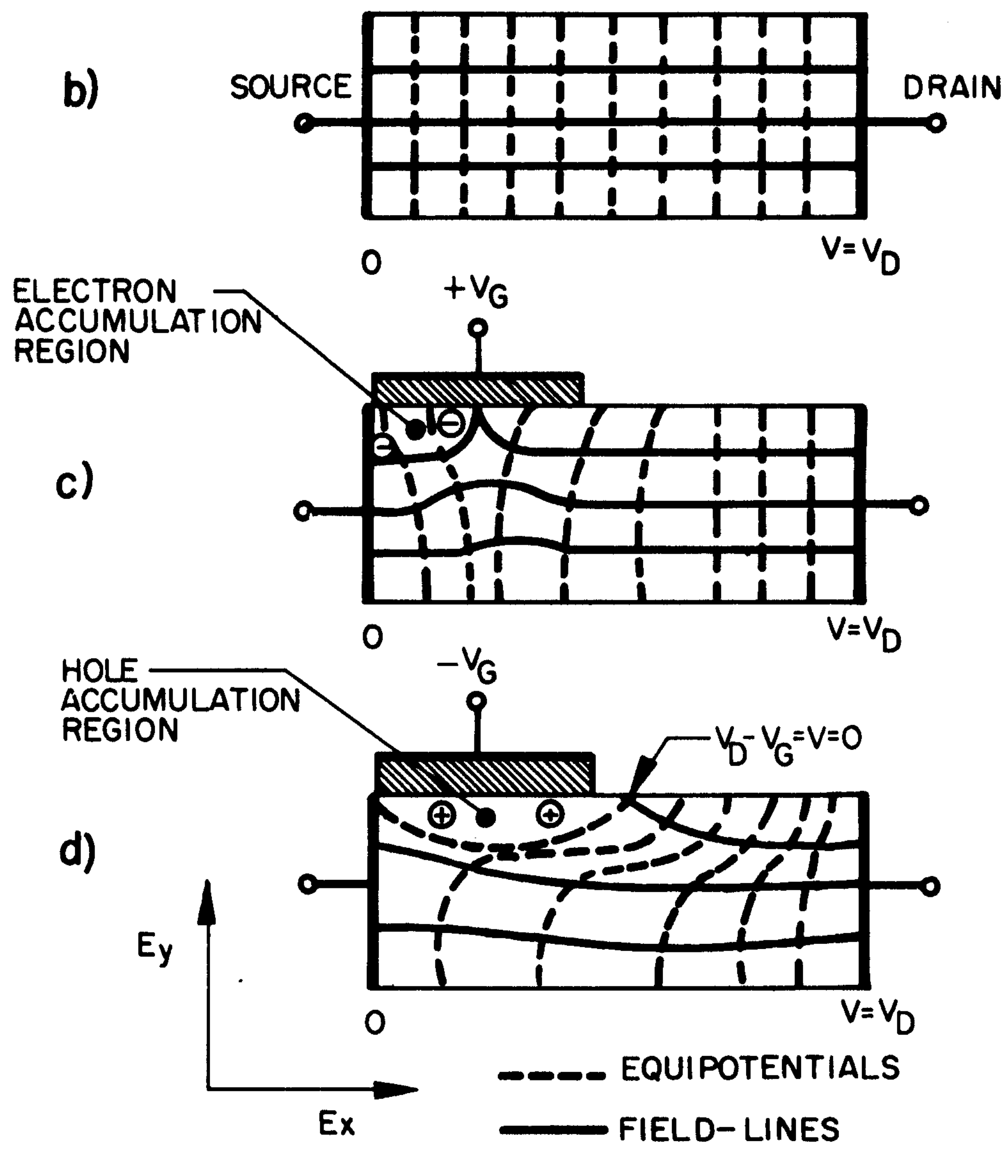


Figure 30

where

q = electron charge

N_A = acceptor impurity density

L_D = distance between source and drain

ε_s = relative dielectric constant of the semiconductor

Besides the depletion mode of operation with a negative gate bias at the gate, the enhancement mode operation with a positive gate bias is possible. A positive bias enhances the potential distribution around the source PN^+-junction, thus increasing the drain current. These two different modes of operation can be understood, when examining the field maps in Figure 30 where

<u>30b</u> pertains to normal case of current flow between source and drain and no disturbance from the gate electrode is present

<u>30c</u> pertains to the positive gate enhancement mode of operation, where the electric field is increased in the region near the source

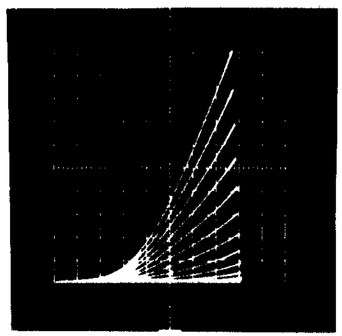
<u>30d</u> pertains to the negative gate (depletion) mode of operation, where the electric field is decreased in the region near the source.

The two modes of operation have been experimentally verified and typical characteristics are shown for both types in Figure 31, which also indicates the excellent temperature performance of this type of device down to liquid nitrogen and possibly cryogenic temperatures.

Evidence of the space-charge-limited current behavior was obtained first on a MOS-TFT made on a silicon film grown on sapphire with a P-type resistivity of 150 Ωcm. The device exhibits mixed characteristics since its geometry is not optimized for SCL-triode operation. At low voltages the normal operation characteristics of the MOST are observed, identified as region I and II in Figure 32. Above the onset voltage, V_{ON}, space-charge-limited current is additive to the drain saturation current I_{DS}. In region III, punch-through has occured and two current components, namely I_1, and I_2, are present. One current component is caused by electrons flowing in the channel and the other by electrons flowing under space-charge-limited condition in the depleted P-film region. Eliminating, therefore, the current component in the channel by recessing the

VOLTAGE-CURRENT CHARACTERISTICS OF THIN-FILM SPACE-CHARGE LIMITED TRIODES (SILICON ON SAPPHIRE)

POSITIVE GATE VOLTAGE OPERATION
(Cut-Off at V_G = O)

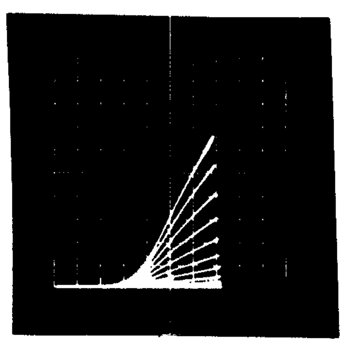


V_G = +12V

Temp = 300°K

V_G = O

DEVICE NAS 2-9



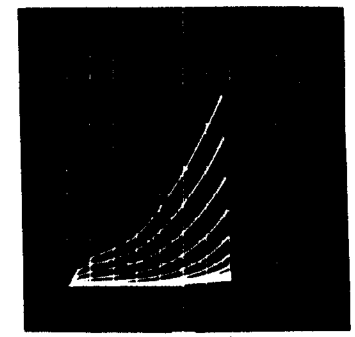
V_G= +12V

Temp = 77°K

V_G = O

IDENTICAL SCALES:
Vert. I_D in 0.5 mA/DIV.
Horiz. V_D in 5V/DIV.
Pos. V_G in 1V/STEP

NEGATIVE GATE VOLTAGE OPERATION
(Conducting at V_G = O)

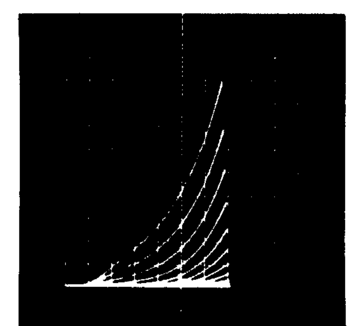


V_G = O

Temp = 300°K

V_G = -12

DEVICE NAS 3-7



V_G = O

Temp = 77°K

V_G = -12V

IDENTICAL SCALES:
Vert. I_D in 0.5 mA/DIV.
Horiz. V_D in 5V/DIV.
Neg. V_G in 1 V/STEP

Figure 31

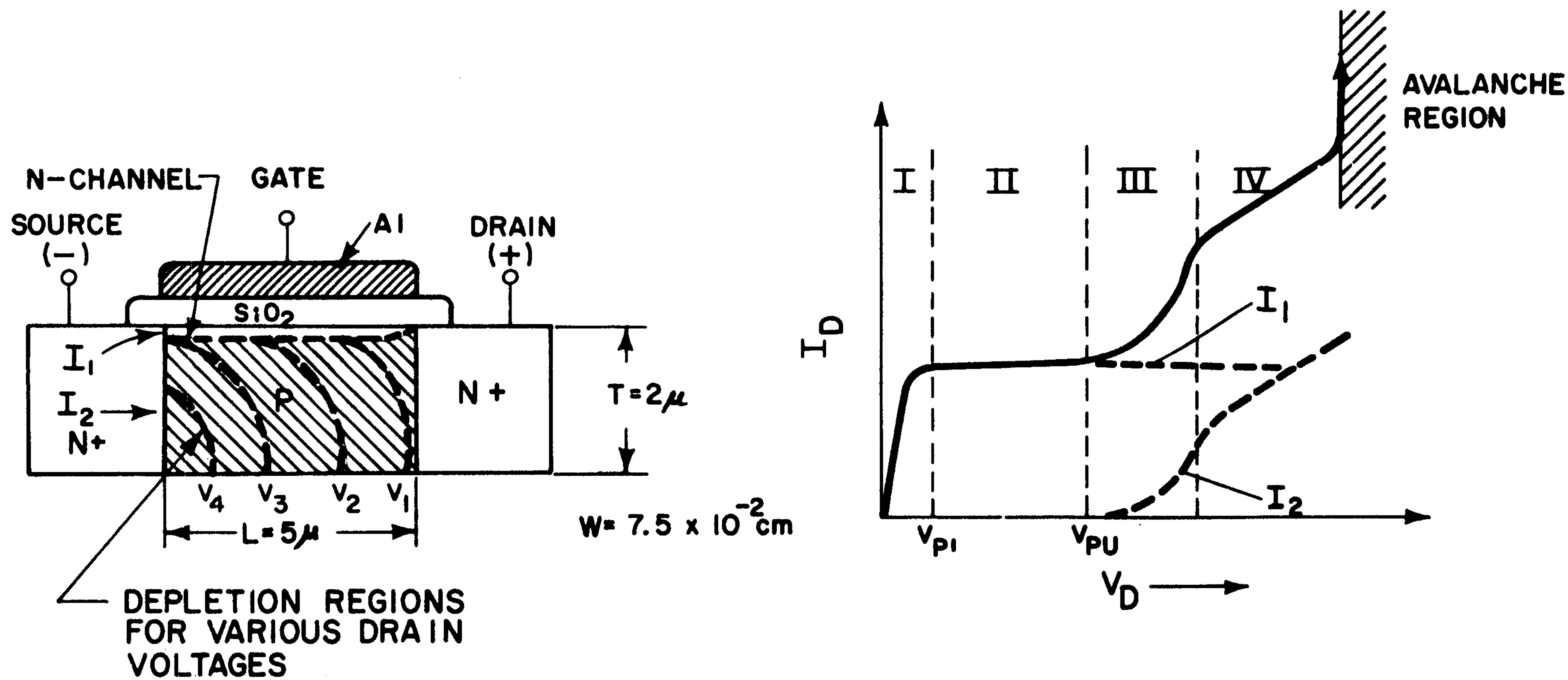

N-CHANNEL
GATE
SOURCE
(−)
Al
DRAIN
(+)
SiO2
I1
I2
N+
P
N +
T=2μ
V4
V3
V2
V1
L=5μ
W= 7.5 x 10^-2 cm
DEPLETION REGIONS FOR VARIOUS DRAIN VOLTAGES
AVALANCHE REGION
I
II
III
IV
ID
I1
I2
VPI
VPU
VD

Figure 32

gate electrode, will lead to the structure of the proposed thin-film SCL-triode as shown in Figure 29, which employs the dielectric gate structure. The operation of a narrow gate MOS-Transistor, e.g. small L_D, as a space-charge-limited triode with full gate covering source and drain channel region was described by Atalla[26]. The additive current component can also possess a linear relation, which is indicative of space-charge-limited current, whereby the electrons reach their high drift field limiting velocity. In region IV the additive current to I_{DS} is equal to

$$I_{SCL} = \frac{2\varepsilon\varepsilon_o v_{lim} \; A}{L^2} \quad V_D \text{ at } V_D >> V_{ON} \tag{50}$$

In region III:

$$I_{SCL} = \frac{9\varepsilon\varepsilon_o \; \mu A}{8 \; L^3} \quad V_D^{\;2} \text{ at } V_D > V_{ON} \tag{51}$$

In region II $\quad (I_{SCL} = O)$:

$$I_{DS} = \frac{\mu \; C_g}{2L^2} \quad (V_G - V_o)^2 \quad \text{at } V_D < V_{ON} \tag{52}$$

In region I $(I_{SCL} = O)$:

$$I_D = \frac{\mu \; C_g}{L^2} \quad \left[(V_G - V_O) \; V_D - \frac{V_D^{\;2}}{2} \right] \tag{53}$$

A typical $V_D I_D$ - characteristic of MOS-TFT with a P silicon-on-sapphire structure is shown in Figure 33. It shows clearly the behavior in the four current regions as described by above equations. Above 45 volts avalanche breakdown occurs.

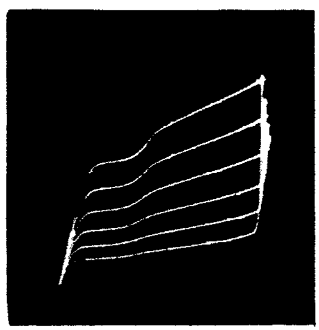
The space-charge-limited current characteristics of MOS-Transistors were theoretically predicted by Geurst[27] in the case for large values of V_D and small values of L_D/h. This approach of solving the voltage-current characteristic of the insulated-gate field-effect transistor could be used to derive the voltage-current characteristics of these devices, since it takes in consideration

V_D I_D - CHARACTERISTIC OF MOS-TFT

P SILICON -ON- SAPPHIRE STRUCTURE

Si Film Thickness	5000 Å
SiO_2 - Gate Oxide	1000 Å
Channel Length	L = 10μ
Channel Width	W = 700μ

N - Channel Enhancement Mode Operation



Scales:

Vertical I_D in 0.2 mA/DIVISION

Horizontal V_D in 5V/DIVISION

Increasing positive gate bias in 1V/STEP

Figure 33

the x and y components of the fields E as indicated in Figure 30. This of course requires a solution of Poisson's equation in two dimensions to the appropriate boundary conditions and should be subject of a theoretical study. One can assess the voltage-current characteristics of the space-charge-limited triode with dielectric gate by a charge-control analysis, with emphasis on transit-time effects under drift condition. The results of this analysis will be of first order, but are shown to correlate well with experimental data on actual devices. With this analysis, one can show, that the fundamental limitation of all charge control type devices is the transit-time of electrons between source and drain. In the space-charge-limited triode, the space-charge is determined by the drain-to-source voltage, V_D. This is in direct contrast to the normal MOS-Transistor with pentode-like characteristics, where the space-charge is determined primarily by the gate potential, V_G, alone at $V_D > V_G$. The basic operation of the device in the structure of Figure 29 can be explained through the sketches of the field-line plots were published for a dielectric triode by Vine and Franks(28) using a resistance-network analogue technique. However the present geometry was not considered and only structures based on plane parallel-sided configuration were treated. After punch-through is reached at a drain voltage V_D larger than V_P, space-charge-limited current of electrons will occur across the P-region with length L_D. This current is voltage dependent through V_D and can be effectively modulated by applying a negative or positive gate-voltage V_G. As a consequence of this applied voltage, a retarding or aiding field is set up between the gate terminal and source current plane, which decreases or increases the transit-time for electrons through the P-region of the length L_D.

In the following analysis, it is assumed that the thermally generated carriers are negligible and the semiconductor is trap-free and the space-charge introduced from the gate voltage is negligible in comparison to the present space-charge setup by the drain voltage. The drain current is then defined by

$$I_D = \frac{Q_D}{\tau_{eff}} \tag{54}$$

Where $Q_D = C_D V_D$ is the charge controlled by the drain voltage, V_D and C_D is the space-charge capacitance. With no gate bias the effective transit-time for electrons from source to drain is equal to

$$\tau_D = \frac{L_D^2}{\mu_o V_D} \tag{55}$$

so that the drain current is equal to

$$I_D = \frac{\mu_n C_D}{L_D^2} V_D^2 \tag{56}$$

Equation 56 gives the relation for space-charge-limited current between source and drain plane, with neglect of the usual numerical factor of 9/8. With applied gate bias, one can define an effective transit-time

$$\tau_{eff} = \frac{\tau_D \tau_G}{\tau_D + \tau_G} \tag{57}$$

where

$$\tau_G = \frac{L_G^2}{\mu_n V_G} \tag{58}$$

Combining Equations 54, 55, 57, and 58, yields the drain current as function of V_D and a positive V_G, in the form

$$I_D = \frac{\mu_n C_D}{L_D^2} (V_D + V_G)^2 \left[1 + \left(\frac{L_D}{L_G}\right)^2 \frac{|V_G|}{(V_D - V_G)} \right] \tag{59}$$

For the negative gate voltage operation

$$I_D = \frac{\mu_n C_D}{L_D^2} (V_D - V_G)^2 \left[1 - \left(\frac{L_D}{L_G}\right)^2 \frac{|V_G|}{(V_D - V_G)} \right] \tag{60}$$

As a consequence of the assumptions, it should be noted that in the positive gate bias operation the triode reaches a limiting current value at high V_G values of

$$I_D = \frac{\mu_n C_D}{(L_D - L_G)^2} V_D^2 \tag{61}$$

This means physically that the source plane has been moved to the edge of the gate electrode (see Figure 29), so that the gate voltage becomes rather ineffective in modulating the space-charge-limited current commencing between a plane at the gate edge and the drain. Figure 34 is an experimental verification of this case. At positive gate voltages above 10 volts, crowding is observed, which means loss of modulation control. The envelope of the limiting current gives a square-law characteristic as expected from Equation 61. In the intermediate ranges of positive gate voltage the transconductance is obtained from Equation 59 by differentiation in respect to V_G and gives

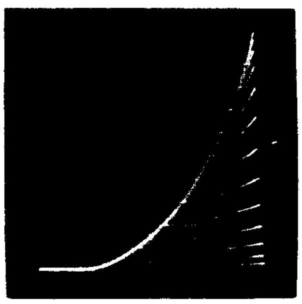
$$g_m = \frac{d I_D}{d V_G} = \frac{\mu C_D}{L_D^2} \left\{ V_D \left[2 + \left(\frac{L_D}{L_G} \right)^2 \right] + 2 V_G \left[\left(\frac{L_D}{L_G} \right)^2 + 1 \right] \right\} \tag{62}$$

The transconductance has according to Equation 62 a linear dependence on V_G, which can be observed on the experimental device NAS 2-9 in Figure 31. At low gate voltages, the built-in voltage, V_o, will contribute to deviations from the relation in Equation 62. This voltage is determined by the excess charges residing in the SiO_2 dielectric and at Si-SiO_2 interface. It should be also noted that drain current will only flow when $V_D > V_P$. This condition causes a linear shift of the voltage-current characteristic equal to V_P, since below this voltage no space-charge is present, which can be modulated by the gate potential. For effective triode operation, it is desirable to have low punch-through voltages, which can be obtained according to Equation 49, by high resistivity P-type material, e.g. low N_A, and small dimensions for L_D. In the devices investigated, $L_D = 10\mu$, so that with a P-type resistivity of 100 to 200Ωcm, the values for V_P are between 5 and 10 volts. For $L_D = 5\mu$, one would obtain, with the same resistivity, values between 1.25 and 2.5 volts.

V_D I_D - CHARACTERISTIC OF SCL-TRIODE

(P Silicon-on-Sapphire Structure)

Si Film Thickness	1μ
SiO_2 - Gate Oxide	1000 Å
Channel Length	$L_D = 10\mu$
Channel Width	$W = 625\mu$
Gate Width	$L_G = 5\mu$



Device NAS 4-1

Scales:

Horizontal V_D in 10V/DIV.

Vertical I_D in 1mA/DIV.

Positive Gate in 1V/STEP

Figure 34

The voltage-current characteristic of the SCL-triode by including V_o can be derived by replacing the transit-time in Equation 55 with the modified value due to V_o and putting

$$\tau_D = \frac{L_D^{\,2}}{\mu_n (V_D + V_G - V_o)} \tag{63}$$

yields

$$I_D = \frac{\mu_n C_D}{L_D^{\,2}} \left[(V_D + V_G - V_o)^2 + \left(\frac{L_D}{L_G}\right)^2 (V_D + V_G - V_o)(V_G - V_o) \right] \tag{64}$$

Note that Equation 59 and 64 represent a different functional relationship than that proposed by Wright(1) based upon a modified vacuum triode approach. The transconductance, which is the derivative of Equation 64 in respect to V_G is now

$$g_m = \frac{\mu_n C_D}{L_D^{\,2}} \left\{ V_D \left[2 + \left(\frac{L_D}{L_G}\right)^2 \right] + 2\,(V_G - V_o) \left[1 + \frac{L_D}{L_G}^{\,2} \right] \right\} \tag{65}$$

and reveals the correct dependence on V_G as observed experimentally. When the device is operated with a negative gate potential it has a transconductance of

$$g_m = (-)\,\frac{\mu_n C_D}{L_D^{\,2}} \left\{ V_D \left[2 + \left(\frac{L_D}{L_G}\right)^2 \right] - 2V_G \left[1 + \left(\frac{L_D}{L_G}\right)^2 \right] \right\} \tag{66}$$

which was obtained by differentiation of Equation 60 in respect to V_G. For the negative gate voltage operation the triode has a cut-off condition, which occurs at a gate voltage

$$V_{GCO} = \frac{V_D}{1 + \left(\frac{L_D}{L_G}\right)^2} \tag{67}$$

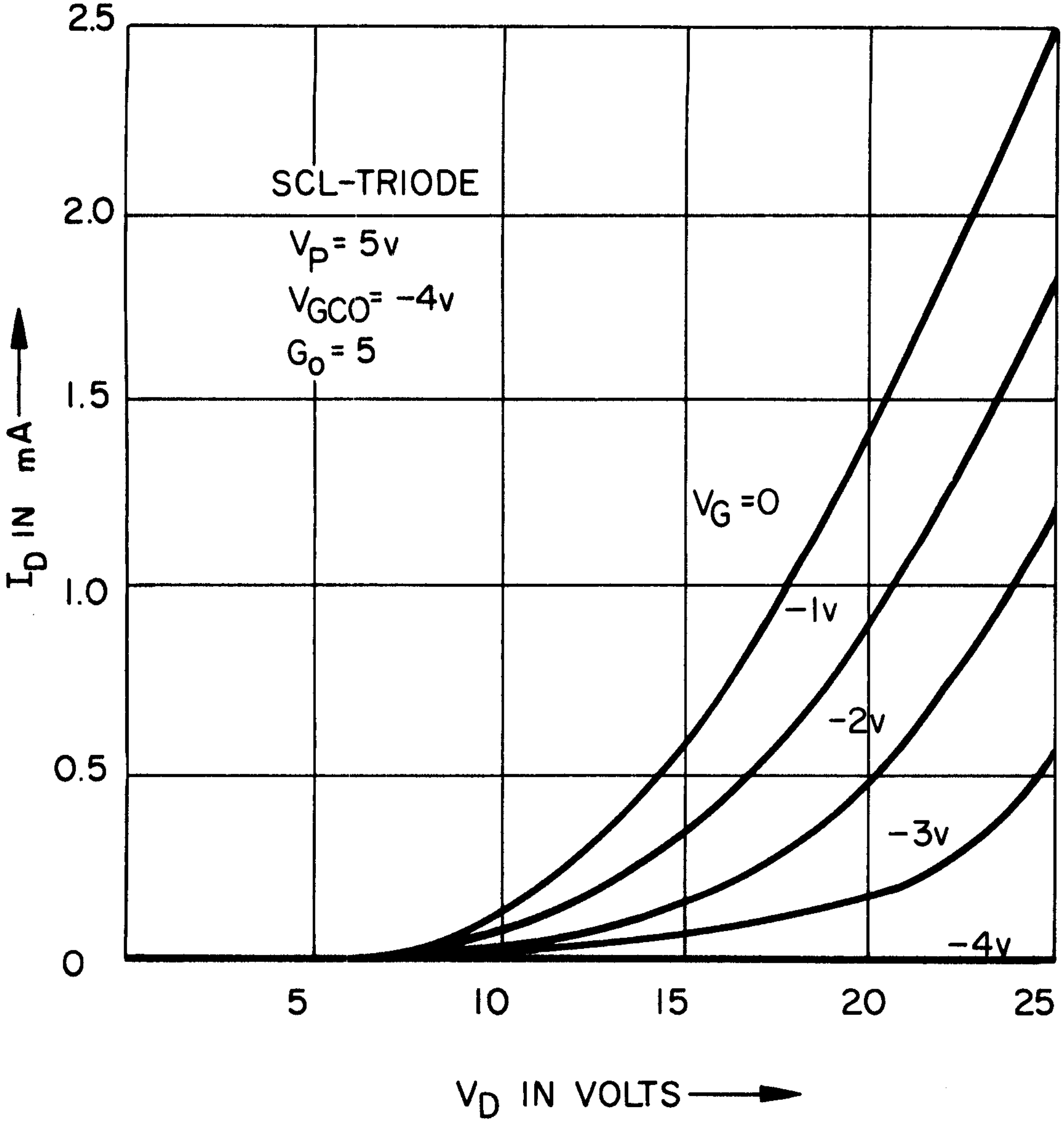
The amplification factor, G_o, of the triode at cut-off is therefore

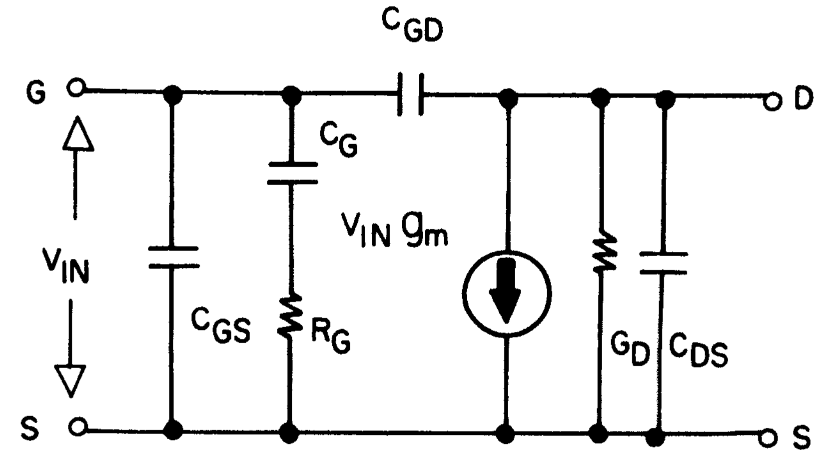
$$G_o = \frac{V_D}{V_{GCO}} = 1 + \left(\frac{L_D}{L_G} \right)^2 \qquad (68)$$

Although the transit-time concept gives a correct functional relation of the current-voltage characteristic as function of the geometric ratio L_D/L_G, which determines the amplification factor G_o of the device, it is recognized intuitively, that also the ratio of L_D/h should have an important contribution. This functional relation will be established, when a two dimensional solution to Poisson's equation is available.

A numerical example will demonstrate the good correlation of the first order theory with experiment within a factor of two, which is very good in view of the uncertainties of some parameters. The parameters apply to the structure of device NAS 3-7, whose voltage-current characteristics are shown in Figure 31. The nominal dimensions for $L_D = 10 \times 10^{-4}$cm, $L_G = 5 \times 10^{-4}$cm, and $W = 6.25 \times 10^{-2}$cm. Equation 60 is plotted in Figure 35 using the following other parameters: $\varepsilon_s = 12$ (Si), $\varepsilon_i = 4$ (SiO_2), $h = 1 \times 10^{-4}$cm, $\mu_n = 1000$cm^2/Vsec and $V_P = 5$ volts. The theoretical amplification factor from Equation 68 is equal to 5 and although the experimental device shows, that I_D at $V_G = O$ and V_{GCO} is twice the calculated value, the experimental amplification factor is about 5 and shows a remarkably good agreement with Equation 68, when considering only the geometrical parameters L_D and L_G. The first order theory for the voltage-current characteristic can therefore be used with confidence to assess the performance of an improved space-charge-limited triode. The relation given in Equation 59, and 60 reveals that:

a) For more effective modulation, L_G should be much smaller than L_D, so that L_D/L_G becomes large. In the geometries presently investigated the best ratio is 2, with $L_D = 10\mu$ and $L_G = 5\mu$. Further refinements in photolithographic techniques may achieve in the near future a ratio of 5, which would result in an amplification factor $G_o = 26$.





PI-SECTION EQUIVALENT
CIRCUIT OF SCL-TRIODE

Figure 35

b) The punch-through voltage, V_P, should be made as low as possible, which requires high resistivity heteroepitaxial silicon film growth on sapphire or other suitable high temperature single-crystal substrates.

Experimental devices have confirmed the two modes of operation and photographs of electrical characteristics at room temperature, e.g. 300°K and liquid nitrogen temperature, e.g. 77°K are shown in Figure 31. It is interesting to notice, that leakage current components disappear at the low temperature, since "freeze out" of carriers takes place below 100°K. The remaining carriers are believed to be "hot" electrons. In the display, straight line portions can be seen, which are indicative of space-charge-limited currents under velocity saturation. Solving Poisson's equation by assuming that the charge carriers move with constant velocity - here the limiting velocity v_{lim} of electrons at high fields - predicts the relations as given previously by Equation 50

$$I_D = \left(\frac{2\varepsilon_s \varepsilon_o \, v_{lim} \, A}{L_D^2} \right) V_D \tag{69}$$

The critical field in silicon for electrons to reach their limiting velocity is about 2×10^4 V/cm. Since in our structure $L_D = 10 \times 10^{-4}$ cm, at $V_D = 20$ V this critical field is established and will be exceeded at higher voltages.

The general frequency characteristics and the frequency limitations have been obtained from a set of Y-parameter measurements as a function of frequency using the General-Radio Admittance and Transfer-Function Bridge. The measurements of a space-charge-limited triode (NAS 2-9) operating with positive gate bias are shown in Figure 36. From these measurements the π -section equivalent circuit has been derived, which is shown in Figure 35. The measurements and the equivalent circuit can be represented by the following set of Y-parameters ($\omega = 2\pi f$)

$$Y_{11} = \frac{1}{R_G} \left(\frac{\omega}{\omega_o} \right)^2 + j\omega \left[C_{GS} + C_{GD} + \frac{C_G}{1 + \left(\frac{\omega}{\omega_o} \right)^2} \right] \tag{70}$$

$$Y_{12} = -j\omega \; C_{GD} \tag{71}$$

$$Y_{21} = \frac{g_m}{1 + \left(\frac{\omega}{\omega_o}\right)^2} - j\omega \left[C_{GD} + \frac{g_m/\omega_o}{1 + \frac{\omega}{\omega_o}^2} \right] \tag{72}$$

$$Y_{22} = G_D + j\omega \; (C_{GD} + C_{DS}) \tag{73}$$

For the equivalent cirucit and the actual device, the following three characteristic frequencies can be defined from Equation 70, 71, and 72

$$\omega_o = (R_G \, C_G)^{-1} \tag{74}$$

$$\omega_c = \frac{g_m}{C_{21}} \tag{75}$$

$$\omega_{max} = \frac{g_m}{C_{12}} \tag{76}$$

ω_o is the frequency, where the real part of Y_{21} has dropped to the value of $g_{mo}/2$, where g_{mo} is the low frequency value and $R_G \, C_G$ is the time constant associated with the gate input network. ω_c is the cut-off frequency of the device due to the feedback effect of $C_{21} = C_{GD}$ and ω_{max} is the theoretical maximum frequency of oscillation, which can be realized in practice only, if $\omega_o > \omega_{max}$, but is usually less than the theoretical value due to parasitic circuit elements not properly accounted for in the equivalent circuit. These parasitic elements contribute to losses when the operating frequency of the device approaches its frequency limitation at f_{max}, where the gain has dropped to unity. For the SCL-triode NAS 2-9 in Figure 36, f_c = 300 MHz and f_{max} = 500 MHz. Other devices were measured, which indicated maximum frequency of oscillation as high as 1 GHz. In most cases a premature fall-off in $g_m = Y_{21r}$ was observed,

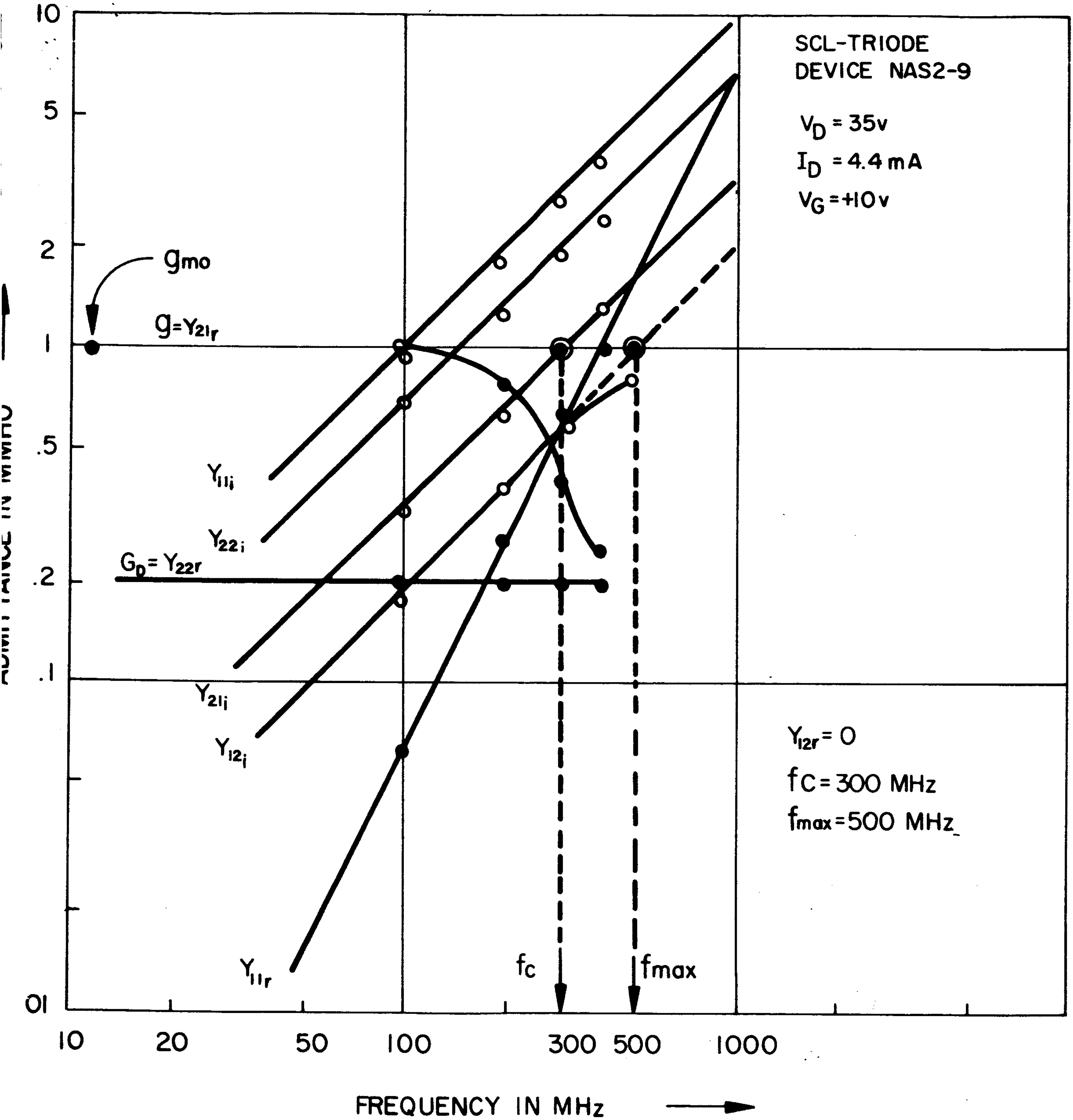

SCL-TRIODE
DEVICE NAS2-9
$V_D = 35v$
$I_D = 4.4 mA$
$V_G = +10v$
g_{mo}
$g = Y_{21r}$
Y_{11i}
Y_{22i}
$G_D = Y_{22r}$
Y_{21i}
Y_{12i}
Y_{11r}
$Y_{12r} = 0$
$f_C = 300$ MHz
$f_{max} = 500$ MHz
f_c
f_{max}
10
5
2
1
.5
.2
.1
01
10
20
50
100
300
500
1000
FREQUENCY IN MHz

Figure 36

which is believed to be caused by a parasitic series resistance in the gate circuit and is not shown in the equivalent circuit of Figure 35. Its probable origin is the thermocompression bond to the aluminum metallization or the aluminum alloy to the N^+ source region. The device NAS 3-6, which apparently did not have this series resistance, has a flat response of $g_m = Y_{21r} = 2\,mA/volt$ from d-c to above 500 MHz. A set of measured Y-parameters obtained on the GR-Admittance Bridge is presented in Figure 37. The device shows a cut-off frequency

$$f_c = \frac{Y_{21r}\ \omega}{2\pi\ Y_{21i}} = \frac{g_{mo}}{2\pi\ C_{21}} \simeq 800\ \text{MHz}$$

and a maximum frequency of oscillation

$$f_{max} = \frac{Y_{21}\ \omega}{2\pi\ Y_{12i}} = \frac{g_{mo}}{2\pi\ C_{12}} = 1\ \text{GHz}$$

The device has a power gain of 6 db at 500 MHz when matched into 5Ω input and output impedance, which was verified by a voltage gain measurement at 500 MHz with 50Ω terminations. The voltage gain $G = V_{out}/V_{in}$ was about 2, which gives

$$PG_{db} = 20\ \lg\ G = 6\ \text{db at 500 MHz}$$

It should be noted, that susceptances, e.g. imaginary parts, contain also the parasitic capacitances of the T0-5 header, which were obtained from a "dummy" header measurement at 300 MHz and are equal to

$$C_{GS}^{*} \simeq 0.4\ pF$$
$$C_{DS}^{*} \simeq 0.4\ pF$$
$$C_{GD}^{*} \simeq 0.1\ pF$$

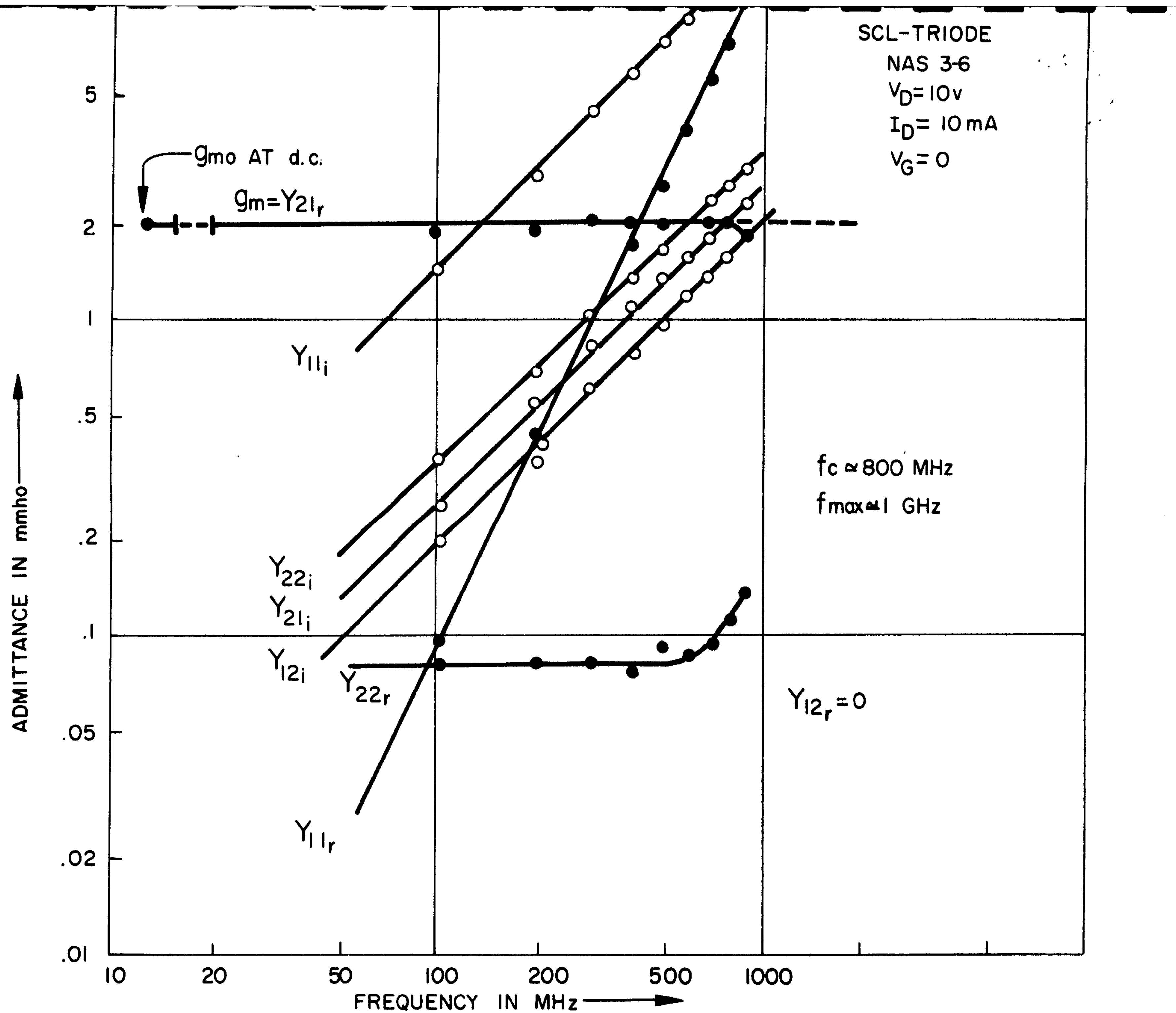

SCL-TRIODE
NAS 3-6
$V_D = 10v$
$I_D = 10 mA$
$V_G = 0$
g_{mo} AT d.c.
$g_m = Y_{21_r}$
Y_{11_i}
Y_{22_i}
Y_{21_i}
Y_{12_i}
Y_{22_r}
Y_{11_r}
$f_c \simeq 800$ MHz
$f_{max} \simeq 1$ GHz
$Y_{12_r} = 0$
5
2
1
.5
.2
.1
.05
.02
.01
10
20
50
100
200
500
1000
ADMITTANCE IN mmho
FREQUENCY IN MHz

Figure 37

The effective and measured capacitances are

$C_{11} = 2.4$ pF

$C_{22} = 0.6$ pF

$C_{21} = 0.48$ pF

$C_{12} = 0.32$ pF

which can be corrected for the parasitic capacitances, so that the actual device has the following values

$C_{11} \simeq 2.0$ pF

$C_{22} \simeq 0.2$ pF

$C_{21} \simeq 0.38$ pF

$C_{12} \simeq 0.22$ pF

These capacitance values predict $f_c \simeq 840$ MHz and $f_{max} \simeq 1.45$ GHz. That ω_o is indeed close to ω_{max} or even greater is concluded from the straight line relation on a log-log scale with a slope of 2 of the admittance vs. frequency plot according to

$$Y_{11r} = \frac{1}{R_G} \left(\frac{\omega}{\omega_o}\right)^2 \tag{77}$$

A higher order theory[29] however, predicts that

$$Y_{11r} = \frac{1}{R_G} \frac{(\omega/\omega_o)^2}{1 + \left(\frac{\omega}{\omega_o}\right)^2} \tag{78}$$

The relation in Equation 78 would not give a straight line plot over a wide range of frequency, unless $\omega/\omega_o < 1$. At the frequency $\omega = \omega_o = \omega_{max}$, Equation 78 would give half the value as predicted from Equation 77.

The power gain of an active device at maximum power output is

$$PG = \frac{|Y_{21}|^2}{2\left[2Y_{11r} Y_{22r} - R(Y_{12} Y_{21})\right]} \qquad (79)$$

where R $(Y_{12} Y_{21})$ represents the real part of $Y_{12} Y_{21}$. Since the real part of Y_{12} is zero in the useful frequency range up to 1 GHz and Y_{11r} Y_{22r} is smaller than $R(Y_{12} Y_{21})$ one obtains from Equation 79 the power gain which is equal to

$$PG = \frac{|Y_{21}|^2}{2 Y_{12i} Y_{21i}} \qquad (80)$$

Inserting the values for $|Y_{12}|$, Y_{12i} and Y_{21i} gives the power gain frequency relation

$$PG = \frac{g_{mo}^2}{2\omega^2 C_{21} C_{12}} + \frac{C_{21}}{2 C_{12}} \qquad (81)$$

If we assume, that $C_{21} = C_{12}$, the power gain is

$$PG = \frac{1}{2} \left[1 + \left(\frac{g_{mo}}{\omega C_{12}}\right)^2\right] \qquad (82)$$

This relation predicts a gain roll-off of 6 db/octave and a maximum frequency of oscillation at PG = 1 of

$$\omega_{max} = \frac{g_{mo}}{C_{12}} \qquad (83)$$

as defined in Equation 76.

2) Discussion and Conclusion

According to the objectives of this contract, the factual data in Section C show the space-charge-limited current operation of the surface gate dielectric triode. The silicon-on-sapphire technique lends itself to the advantageous fabrication of this practical thin-film space-charge-limited triode. Owing to the dielectric isolation of the individual devices, extremely low output and feedback capacitances can be realized and integration of this and other device structures for high speed and high frequency circuits is straightforward.

From the experimental voltage-current characteristics an amplification factor of 5 is determined at the cut-off condition. The reported devices with $W = 625\mu$, $L_D \simeq 8 - 10\mu$, $L_G = 5\mu$ have transconductances in the range of 1 to 2 mA/volt. From a set of Y-parameter measurements a power gain of 6 db is available at 500 MHz and the maximum frequency of oscillation is 1 GHz. The transconductance $g_m = Y_{21r} \simeq 2 \times 10^{-3}$ mho is flat from d-c to about 700 MHz and the feedback capacitance $C_{GD} = C_{12} = 0.32$ pF at 500 MHz (this value includes the parasitic header capacitance of the T0-5 package). The exact voltage-current characteristics of this device as a function of gate voltage requires the solution of Poisson's equation in two dimensions to approximate boundary conditions and is the subject of a theoretical study.

Although the experimental devices are not optimized with respect to the geometrical parameters L_D, L_G, h and t and the material parameters, namely resistivity and mobility, it is concluded, that with refined structures a maximum frequency of oscillation of 2 to 4 GHz can be obtained. Applying the device concept of a recessed gate to the Schottky barrier gate field-effect transistor in GaAs, as described recently by Mead[30], may eventually produce thin-film space-charge-limited triodes in the 5 to 10 GHz frequency range owing to higher mobility. In addition to the excellent temperature and frequency characteristics, the thin-film space-charge-limited triode could exhibit low noise operation according to theoretical investigations by van der Ziel[5].

<u>SECTION D</u>

MATERIAL PREPARATION AND EVALUATION

D) MATERIAL PREPARATION AND EVALUATION

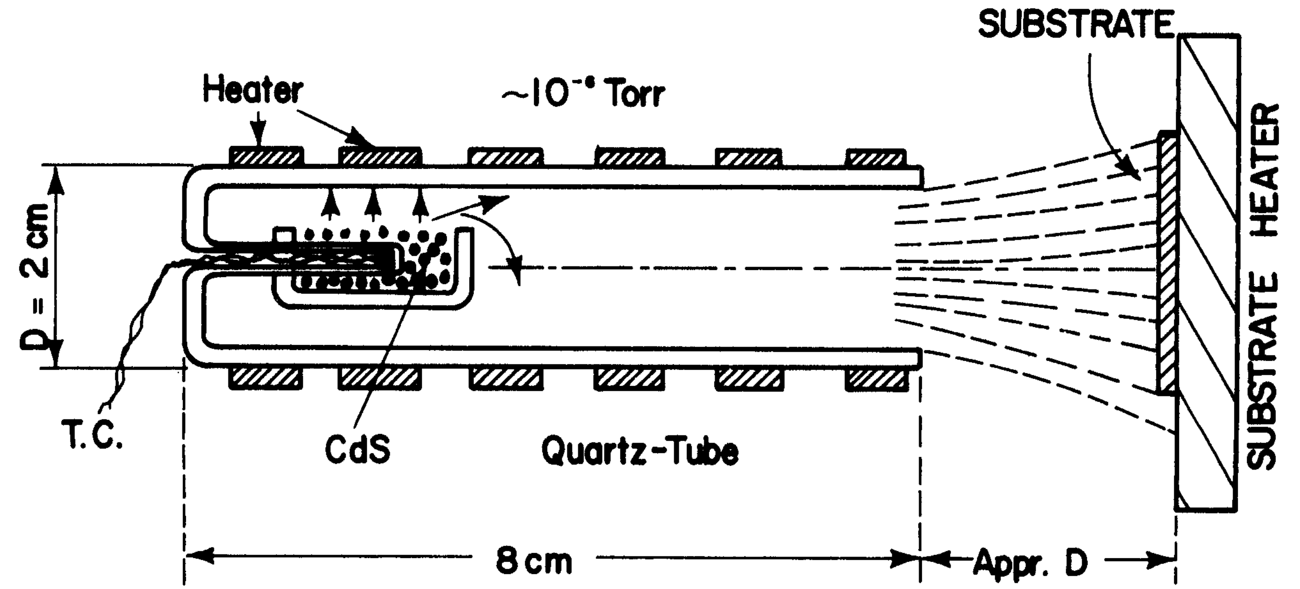
1) CdS Films By Evaporation

The source used for the evaporation of CdS was similar to that described earlier by Zuleeg and Senkovits[31]. A quartz tube about 8 cm long and 2 cm diameter, closed at one end, was uniformly heated from the outside. A thermocouple was embedded into the CdS to monitor the temperature throughout the deposition. The quartz tube was used horizontally in a vacuum bell jar. The substrate, attached to a heater plate, was placed at a distance of about 2 cm from the source orifice. The arrangement is illustrated in Figure 38.

For all CdS evaporations only (111) oriented silicon wafers with a fine polish were used. Immediately before deposition of CdS they were dipped into dilute hydrofluoric acid in order to remove the oxide layer. During the deposition the source was held at a temperature between 550°C and 700°C. The evaporation time in most of the runs ranged from 1 to 5 minutes. In some runs the substrate was heated up to 200°C by means of a heater plate which had been smoothly polished to assure good heat transfer. In other runs the substrate received heat only from the radiating source. The structure of the films obtained did not exhibit much variation from run to run and the films were smooth and adhered quite well to the substrate. The thickness ranged from 0.5 to 2.5μ, depending upon the time of evaporation.

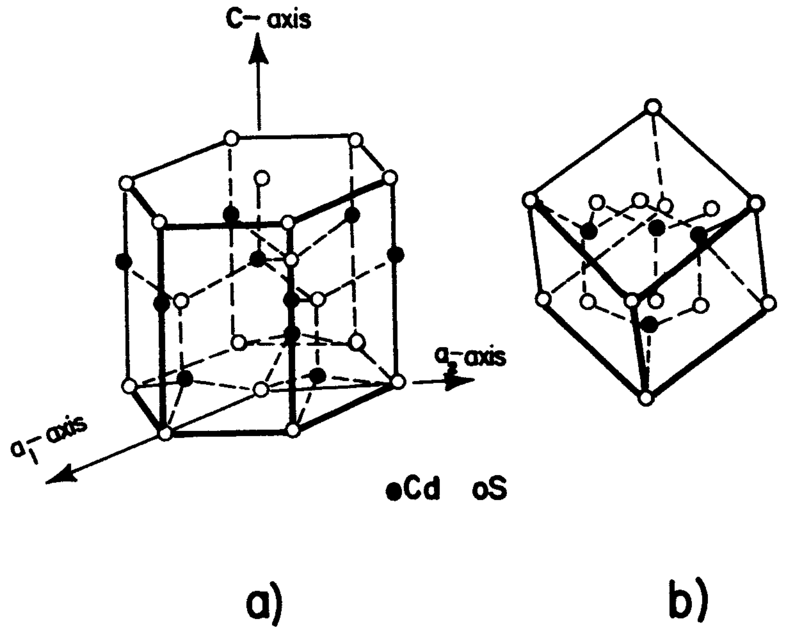
Cadmium sulfide can appear in two modifications. The α phase is the hexagonal wurzite structure, the β phase is the cubic zinc-blende structure as shown in Figure 39. As summarized by Escoffery[32], the hexagonal form seems to be the stable modification between 25 and 900°C. However, when a vacuum deposited CdS film is scraped off the substrate and is powdered, the hexagonal as well as the cubic modification can be found[33], although the formation temperature was well below 900°C.

The Figures 40 through 43 illustrate x-ray diffraction patterns for the samples N-10, N-12, and N-25. These patterns were obtained by using a Norelco wide angle goniometer with a Geiger Müller Counter and 30 V Copper K radiation.

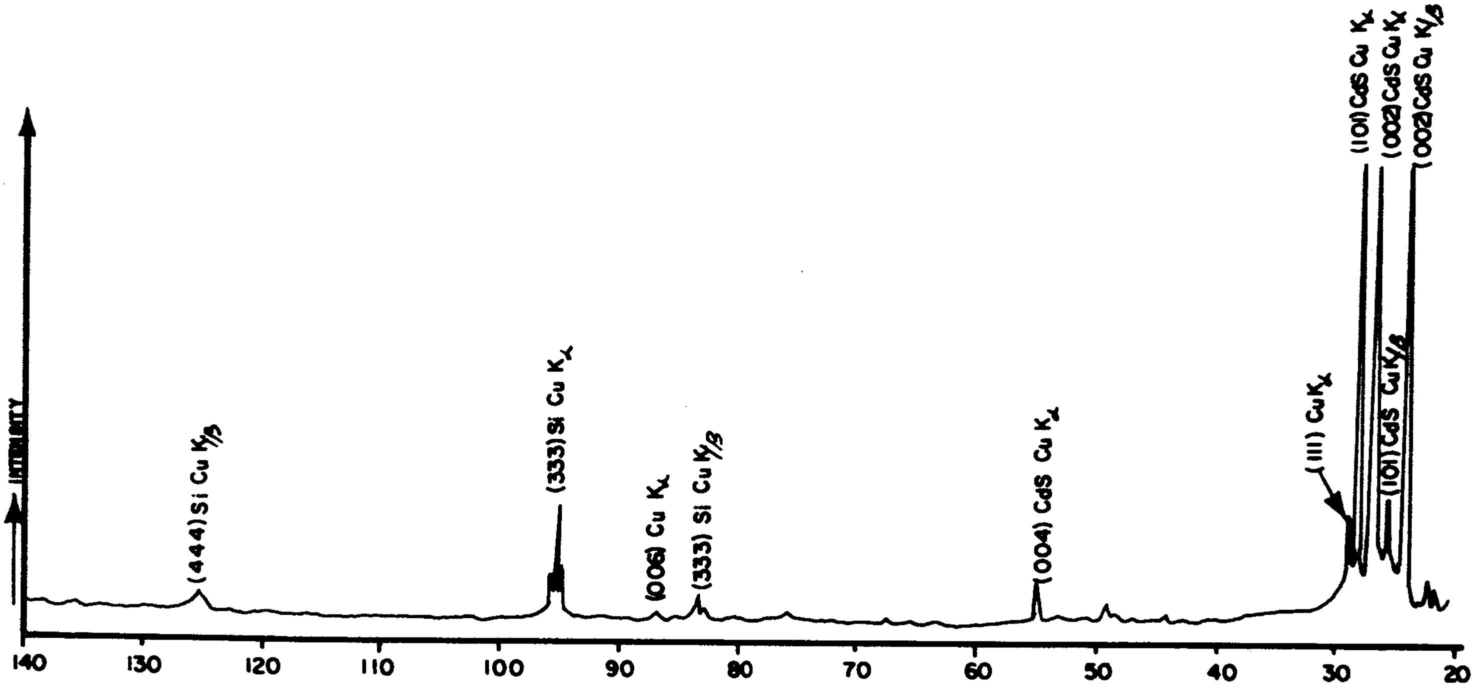


Evaporation Source for CdS.

Figure 38

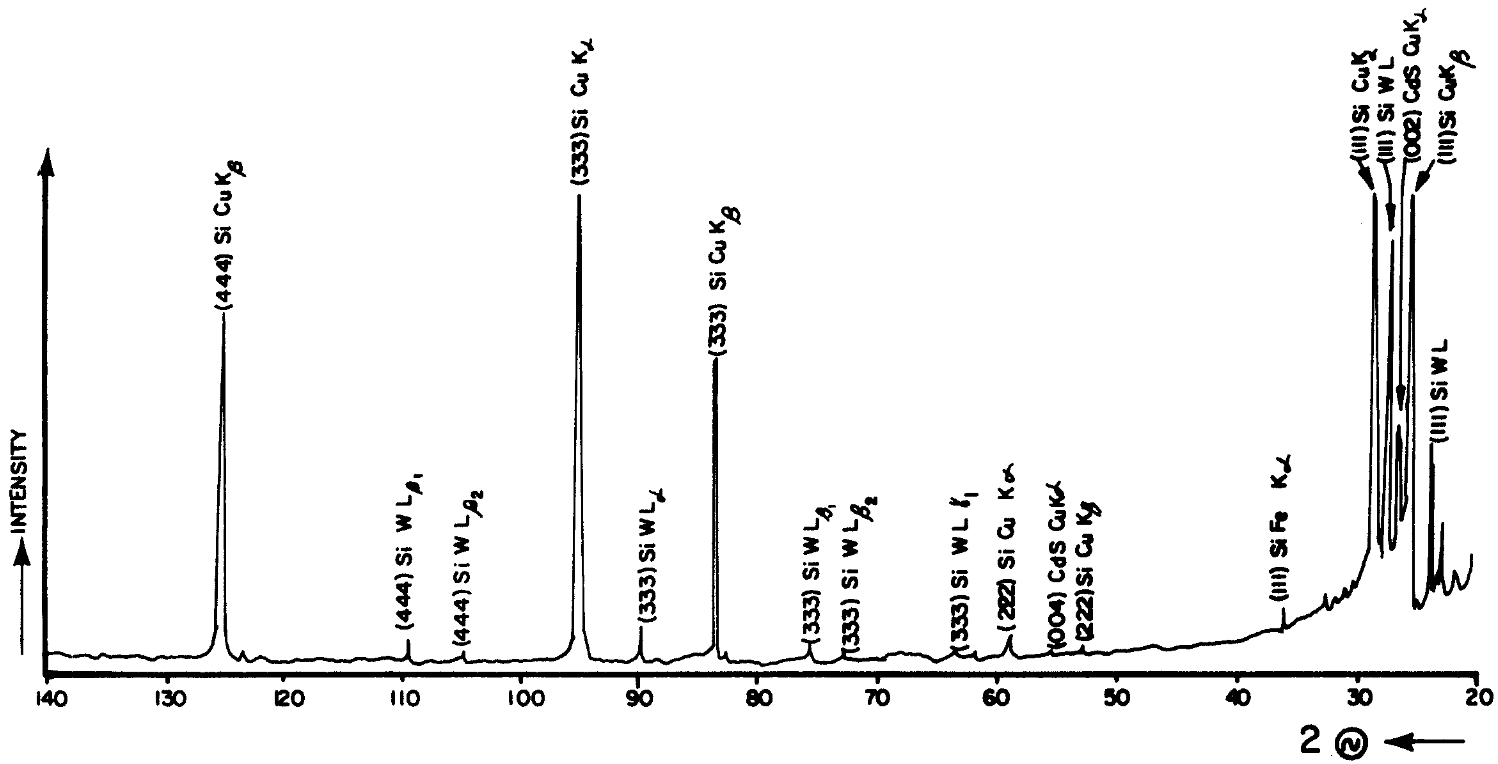


The Crystal Structures of (a) Hexagonal and (b) cubic CdS.



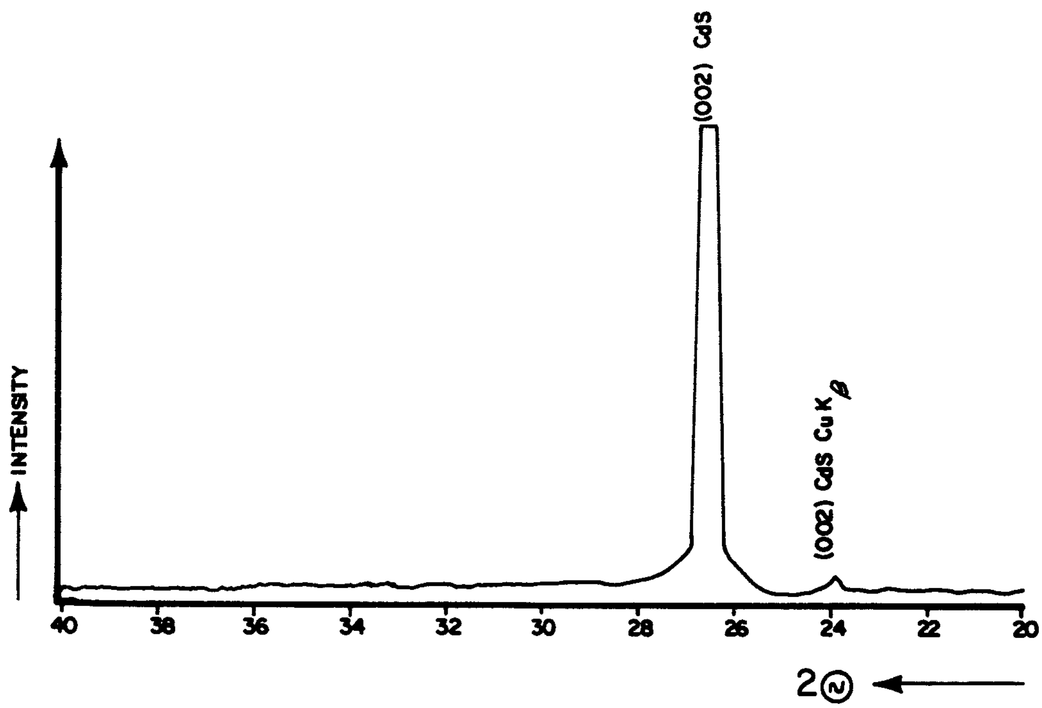
X-Ray Diffraction Pattern of Sample N-10. CdS Evaporated onto a (111) Oriented Silicon Wafer. Five Minutes Deposition with Cold Substrate.

Figure 40



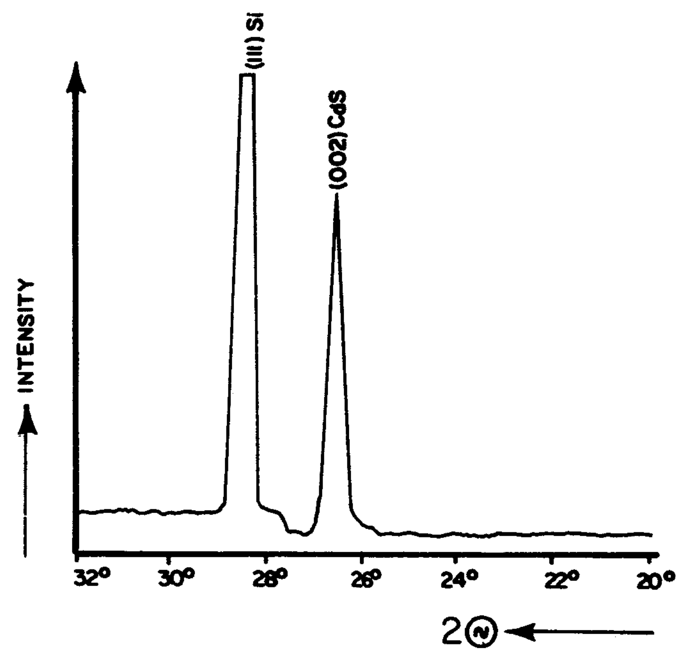
X-Ray Diffraction Pattern of Sample N-12 CdS
Evaporated onto a (111) Oriented Silicon Wafer.
Five Minutes Deposition with Substrate at 110°C.

Figure 41



X-Ray Diffraction Pattern of Sample N-25. CdS Deposited on Unheated (111) Oriented Silicon Wafer.

Figure 42



Pattern of Figure 6 Repeated with Silicon Wafer in Different Position.

Figure 43

The pattern in Figure 40 shows only the (101), (002), and (004) line of CdS plus the silicon lines. Figure 41 is a strongly textured CdS pattern, besides the (002) and (004) peaks of CdS only silicon peaks appear. Figure 42 and 43 are made from the same specimen which was a CdS film on a (111) oriented silicon wafer. In Figure 42 practically the very strong (002) peak of CdS is the only line that can be seen and no silicon line appears. After the wafer was slightly repositioned in the sample holder of the goniometer, the chart of Figure 43 was obtained. Now, the intensity of the (002) CdS reflection is much smaller, but the pattern shows a large (111) silicon peak.

All the CdS x-ray diffractometer patterns obtained showed the (002) reflection to be very strong, other peaks which would normally appear in a powder pattern were either small or could not be identified at all. Patterns of this type indicate a strong preferred orientation of the deposited films. The orientation of a CdS film on a flat silicon substrate apparently is very similar to that on a flat glass plate. A film of CdS evaporated on glass and left untreated, very often is oriented such that the c-axis of most of the crystallites is perpendicular to the surface[31, 34]. This structure results in the large (002) peak in the diffraction pattern. The (002) plane is the most densely packed plane in the wurzite structure and this plane apparently is initially deposited parallel to the flat surface and the film grows from there on attaining a preferred orientation.

The ratio of the intensities of the (111) silicon and (002) CdS peak in the Figures 42 and 43 suggest that the crystallographic orientation of the CdS deposit was not influenced very much by the crystallographic orientation of the substrate. The substrate wafer most likely was cut at a small angle with the (111) plane. The CdS film probably grew in such a manner that the (002) plane was parallel to the smooth substrate surface and was not parallel at the inclined (111) silicon planes. The CdS films apparently show a tendency to orient themselves only with respect to a flat surface, regardless of the crystallographic structure or orientation of the substrate. Since the influence of the substrate orientation upon the growth habit of the layer seems to be very small, it can be assumed that the a-axis of the deposited CdS crystallites are randomly oriented. An epitaxial relationship between substrate and applied layer does not exist.

In Table I, data were compiled for the interpretation of the diffractometer charts. It can be seen that the difference between the d-spacing of the (002) plane of the hexagonal α-CdS and the d-spacing of the (111) plane of the cubic β-CdS is less than 0.1 per cent. Because of this extremely small difference it is not possible to discriminate between the two respective peaks on the chart. The peak marked (002) CdS, therefore, could be attributed to the cubic phase as well. The peak marked (101) CdS, however, is an indication of only the hexagonal phase because in the vicinity of $2\Theta = 28.2°$ there is no reflection of cubic CdS. Hence, from the obtained diffraction patterns alone, no conclusion can be drawn whether the film structure is hexagonal, cubic, or a mixture of both. For the exact determination of the structure, deposited CdS material would have to be scraped off the substrate for a powder pattern examination.

TABLE I

CRYSTALLOGRAPHIC VALUES FOR THE INTERPRETATION OF DIFFRACTOMETER CHARTS

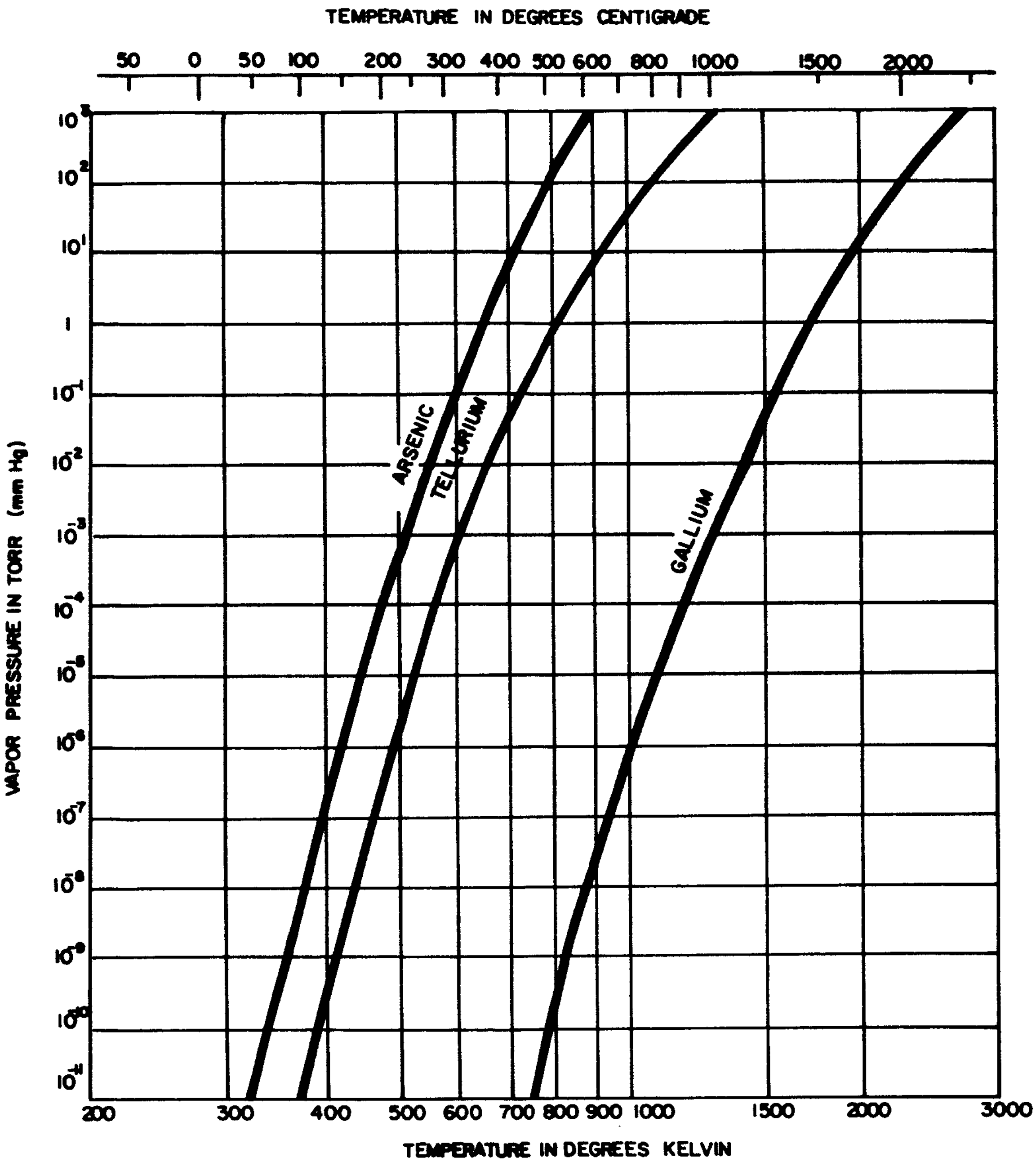
Material	Structures	Plane (hkl)	d-spacing in Å	Line intensity ASTM-card	2Θ with Cu K radiation
α-CdS	hexagonal	(100)	3.583	57%	24.85
β-CdS	cubic	(111)	3.36	100%	26.553
α-CdS	hexagonal	(002)	3.357	59%	26.533
α-CdS	hexagonal	(101)	3.160	100%	28.2
Si	cubic	(111)	3.138	100%	28.44
β-CdS	cubic	(200)	2.2	40%	30.83

2) GaAs Films by The Three Temperature Method

a) Description of the Method:

For the deposition of GaAs the "three-temperature method" was used. This method has been first described by Günther[35, 36] and it has been applied successfully to deposit In Sb[37] and GaAs[38, 39] onto amorphous substrates.

According to this method, gallium and arsenic are evaporated simultaneously from separated crucibles at temperatures T_1 and T_2, respectively. The substrate is heated to the temperature T_3 by means of a special substrate heater. Each of the three temperatures must be held in a certain range to achieve controllable depositions. T_1, the temperature of the gallium crucible, is set at 1200 to 1300°C; the evaporation rate of the gallium governs the growth rate of the GaAs film. The temperature T_2 of the arsenic crucible conveniently is set at about 450°C. This results in an arsenic vapor pressure which is about 100 times greater than that of gallium as can be seen in the graph in Figure 44. The temperature range for the substrate, T_3, is comparatively large. T_3 must be at least as high as the temperature which is required to form the GaAs compound. We found for gallium arsenide deposition on glass substrates that at a substrate temperature below 350°C a silvery, mirror-like deposit was formed. X-ray diffraction analysis of such a film did not reveal any diffraction peaks at all, thus suggesting the deposit to consist of an amorphous mixture of gallium and arsenic. With a substrate temperature higher than 350° the compound GaAs was detectable by x-ray diffraction. This sets a lower limit for T_3. The upper limit is given by the decomposition temperature of the compound. At temperatures of 800 or 900°C GaAs becomes unstable when heated in vacuum because it loses arsenic. In addition, T_3 must be so high that the element with the higher vapor pressure is not deposited in elemental form. When this condition is fulfilled, only the compound is deposited on the substrate. This condition, however, does not present a problem when arsenic is evaporated because of the very high volatility of this element. The arsenic must be evaporated always in excess in order to form the compound GaAs close to stochiometry.



Vapor Pressure of Gallium and Arsenic as a Function of Temperature.

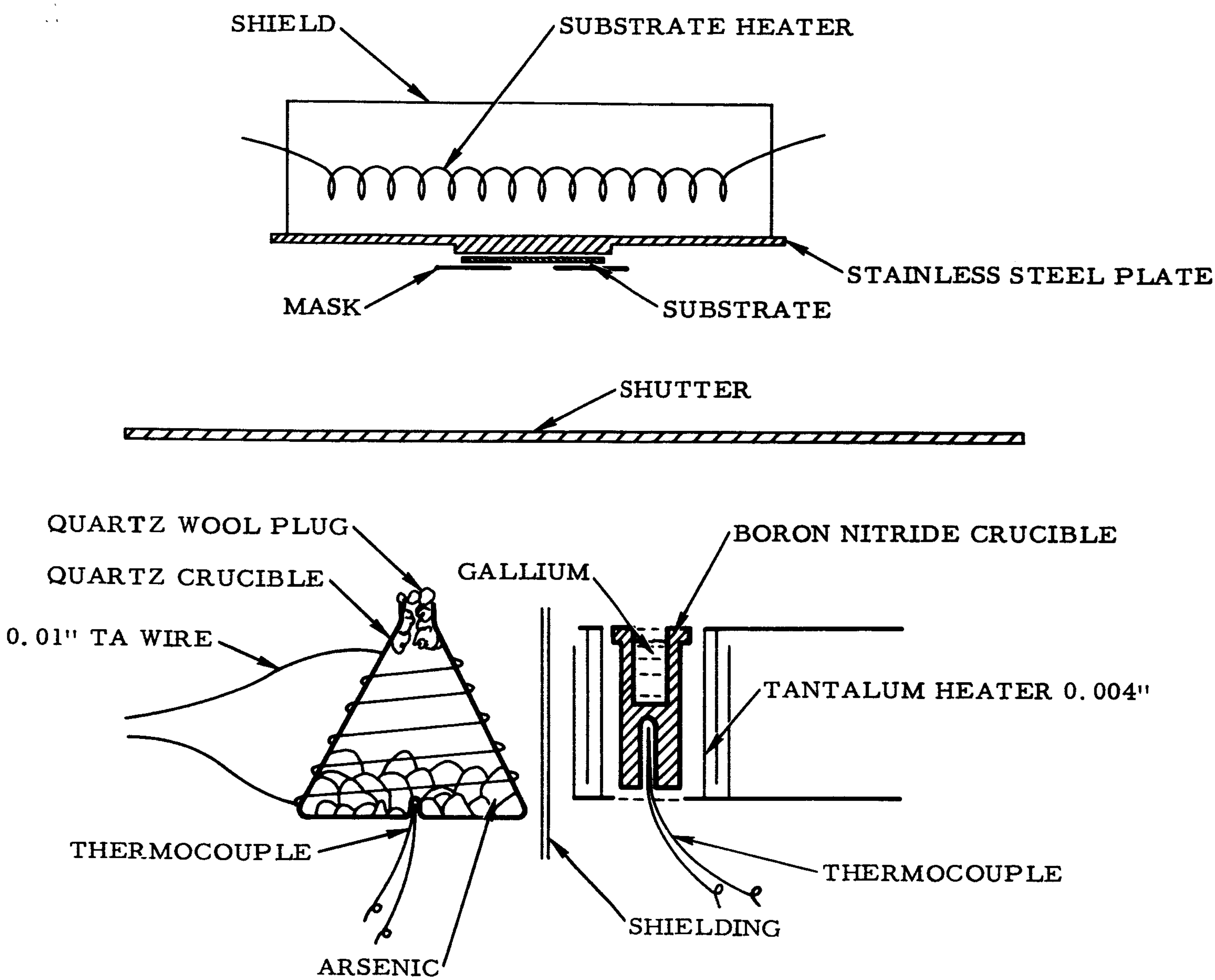
Figure 44

A cross section of the evaporation apparatus for GaAs film deposition with the "three-temperature-method" is illustrated in the Figure 45. Gallium is evaporated from a boron nitride crucible heated by means of a cylinder made of 0.004" thick tantalum sheet metal with a concentric double wall radiation shield. The arsenic crucible is made of quartz glass and heated with a coil of 0.01" tantalum wire. As shown in Figure 45, quartz wool plug is placed into the orifice of the arsenic evaporator as suggested by Howson[39]. Thermocouple wells are provided for both crucibles. A sheet of stainless steel acts as a heat shield between the gallium and the arsenic crucible. The distance between the orifices of the two crucibles is 1.5". A thick stainless steel plate is placed about 2" above the crucibles. The substrate, together with a mask, is held against an elevated section of this plate by means of two rings. The heater coil for the substrate is contained in a metal enclosure which is attached to the steel plate.

Evaporations were performed at a pressure of about 5×10^{-6} torr. The substrates used were silicon and sapphire with different crystallographic orientations and pyrex glass. In some runs tellurium was added to the gallium crucible in order to dope the gallium arsenide film.

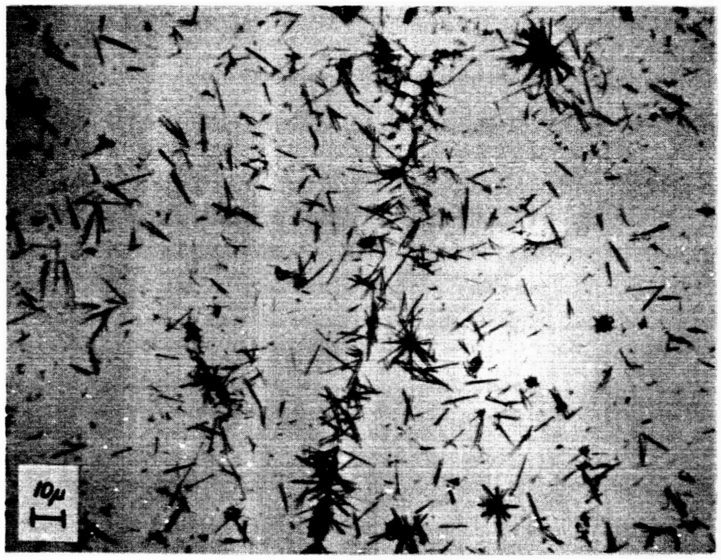
b) Results:

The appearance of the deposited GaAs layers was not very consistent from run to run. The films usually had a mirror-like reflectivity. Sometimes, however, a dark grey haze appeared in certain areas of a substrate wafer. Under the light microscope, it was not possible to clearly identify a structure of the reflecting areas of the GaAs deposits, the surface appeared to be smooth. The hazy areas, on the other hand, often showed a very large amount of tiny, needle-like crystals. These whiskers were up to a few microns thick, protruding in some, but rare cases up to 20μ beyond the otherwise flat surface. Figure 46 is a photomicrograph of a GaAs deposit with whiskers. It can be seen that a certain number of whiskers grow, in some cases, from the same point so that a star is formed. Other irregularities which occasionally were found in the films under the light microscope were small, shiny semispheres which obviously were composed of gallium and which were surrounded sometimes by a dark, solid shell.



SHIELD
SUBSTRATE HEATER
STAINLESS STEEL PLATE
MASK
SUBSTRATE
SHUTTER
QUARTZ WOOL PLUG
QUARTZ CRUCIBLE
0. 01" TA WIRE
GALLIUM
BORON NITRIDE CRUCIBLE
TANTALUM HEATER 0. 004"
THERMOCOUPLE
THERMOCOUPLE
SHIELDING
ARSENIC

Figure 45



GaAs Film with Whisker

Figure 46

The occurrence of whiskers on the films seems to be favored by higher substrate temperatures during the deposition. Furthermore, the quality of the deposits could be improved by using a smaller rate of deposition, e.g. by lowering the gallium crucible temperature. It appeared as if the quartz plug in the outlet of the arsenic crucible, which was not used in the initial experiments, resulted in an improvement of the appearance of the GaAs films because of its baffling action. For all these reasons most of the depositions for the devices were carried out with substrate temperatures below 600°C and with a gallium crucible temperature of approximately 1000°C which resulted in a growth rate of the GaAs films of about 1μ per 20 minutes. Under those conditions the films were shiny and only a few whiskers, if any, could be found.

Apparently the star of whiskers grows on a small droplet of gallium which might have been formed initially. As more and more arsenic is evaporated the liquid gallium is used up to form the needle-like GaAs crystals.

c) Chemical Composition:

The films were synthesized from the elements gallium and arsenic which were both "electronic grade pure". No chemical analysis of these elements was made. From the chemical point of view, the following two properties of the gallium arsenide films are of importance:

i deviation from the stochiometric composition

ii foreign impurities

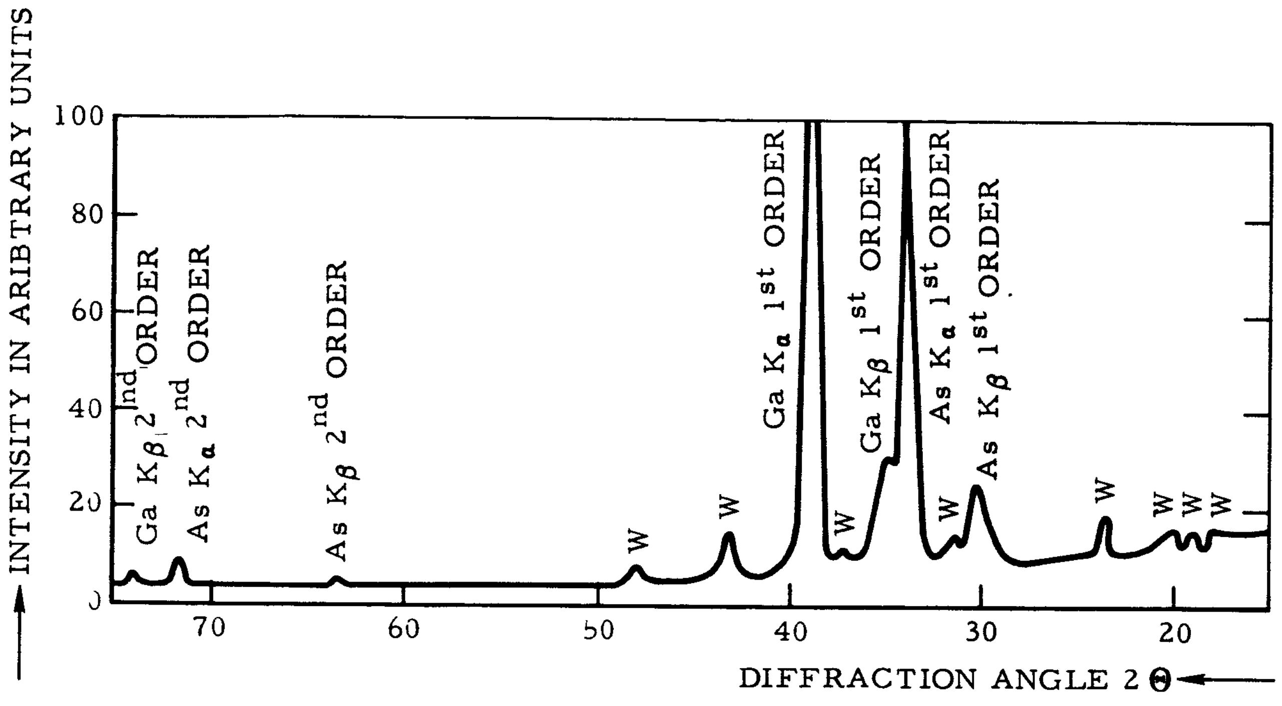
A typical thickness of gallium arsenide films is one micron. This means that in an area of one cm^2 there is not more than about 0.5 mg of material deposited. Such a small quantity of material rules out any wet chemical analysis for an accurate determination of the stoichiometry of the compound. Furthermore, impurities of foreign origin would be far below the detectable limit of this method.

X-ray diffraction analysis made of those films which were deposited at a substrate temperature of 300°C or higher showed the reflections of GaAs corresponding to the values given in the ASTM X-Ray Powder Data File. The lines besides those of the GaAs were always caused by impurity radiation from the x-ray tube. No indication was found for an impurity phase in the film.

Several gallium arsenide films, deposited on silicon as well as on sapphire, have been analyzed with x-ray fluorescence techniques. A Norelco scintillation counter vacuum spectrograph with a lithium fluoride analysing crystal has been used for this purpose. A typical recording is shown in Figure 47 of sample N76-A which is a GaAs film deposited on (111) oriented silicon. The chart was obtained with W-radiation of 40 kV and 25 mA, a scale factor of 32 and a time constant of 2 sec. All the peaks in this and in other recordings could be traced back to either gallium, arsenic or tungsten which stems from the x-ray tube. This means that the concentration of impurity elements with an atomic number of that of aluminum or higher is smaller than the 0.01 to 1 per cent sensitivity limit of the method. For the elements with a lower number than aluminum, particularly oxygen or nitrogen, no conclusion can be drawn because the radiation from these elements is too soft to enter the scientillation counter.

Attempts have been made to obtain information on the stoichiometry of the films by x-ray fluorescence. The accuracy of such a determination depends mainly upon a standard sample which must have the desired composition and the same thickness as the unknown samples. When samples of a compound have the same composition but a different thickness, the ratio of the peak height of a certain line of one constituent to the peak height of the corresponding line of the other constituent will be a function of the sample thickness because the two x-rays with their different energies are affected differently on their way from the point of generation to the sample surface.

Due to the difficulty of the preparation of a proper standard sample, the experiments failed to reveal the stoichiometry of the GaAs deposited with a reasonable accuracy.



INTENSITY IN ARIBTRARY UNITS
100
80
60
40
20
0
70
60
50
40
30
20
DIFFRACTION ANGLE 2 Θ
Ga Kβ 2nd ORDER
As Kα 2nd ORDER
As Kβ 2nd ORDER
W
W
Ga Kα 1st ORDER
W
Ga Kβ 1st ORDER
As Kα 1st ORDER
W
As Kβ 1st ORDER
W
W
W
W

Figure 47

d) Structure Investigation:

The structure of several GaAs films was studied with a Phillips EM-100B electron microscope using conventional replica technique with Pt-Pd and carbon deposition. The films of the samples investigated were deposited at substrate temperatures of 400, 500, 550, and 600°C. The substrates were (111) oriented Si and Ge, and Corning glass 7059. Figure 48 shows the structure of a sample which was deposited at 400°C. The layer seems to be uniformly polycrystalline with a crystallite size of about 500 Å. The picture of the 500°C sample, illustrated in Figure 49, shows a quite different structure. 2000 Å thick clusters, apparently crystallites, are enclosed in a matrix which is similar to that of the previous picture.

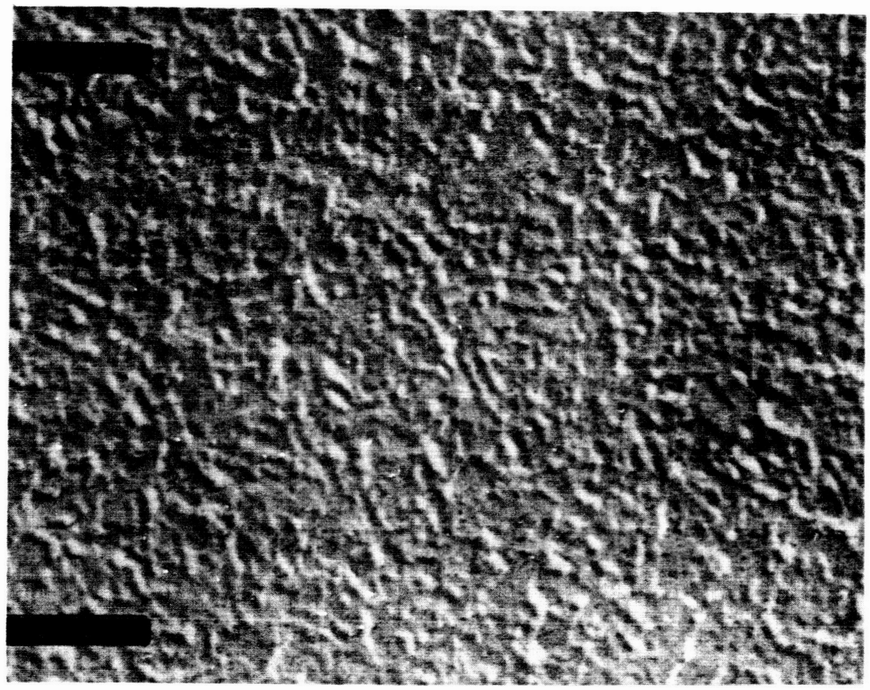
An area without the large particles from the same sample was selected and is shown in Figure 50. The magnification of the electron microscope was brought up to its limit and the markings on this picture indicate a distance of only 0.5μ. The picture reveals a very fine grainy structure. The Figures 51 and 52 show the surface of GaAs films deposited at 550 and 600°C, respectively. Here again comparatively large crystallites of up to 5000 Å diameter are scattered randomly in a relatively smooth layer. The two following, Figures 53 and 54, illustrate the surface of a GaAs film on a germanium and on a glass surface, deposited in both cases with the substrate at 500°C. The structure of the film on germanium is extremely fine and the grains are not larger than a few 100 Å. The film structure on the glass substrate is somewhat coarser. The particles on the glass were in general rougher and higher than those on the germanium as noted by the cast of their shadows.

The electron reflection diffraction pattern of several samples was investigated with the electron microscope. A diffraction pattern, which can be considered typical of that for many other GaAs thin-film specimens, is presented in Figure 55. The picture closely represents a powder pattern. No indication could be found in this picture or in others made under similar conditions for a transition of the continuous rings to discrete points. This means that the crystallite size is well below the diameter of the electron beam which might be between one and five microns. This finding confirms the conclusion about the crystallite size drawn from the replica pictures. It was not possible to determine

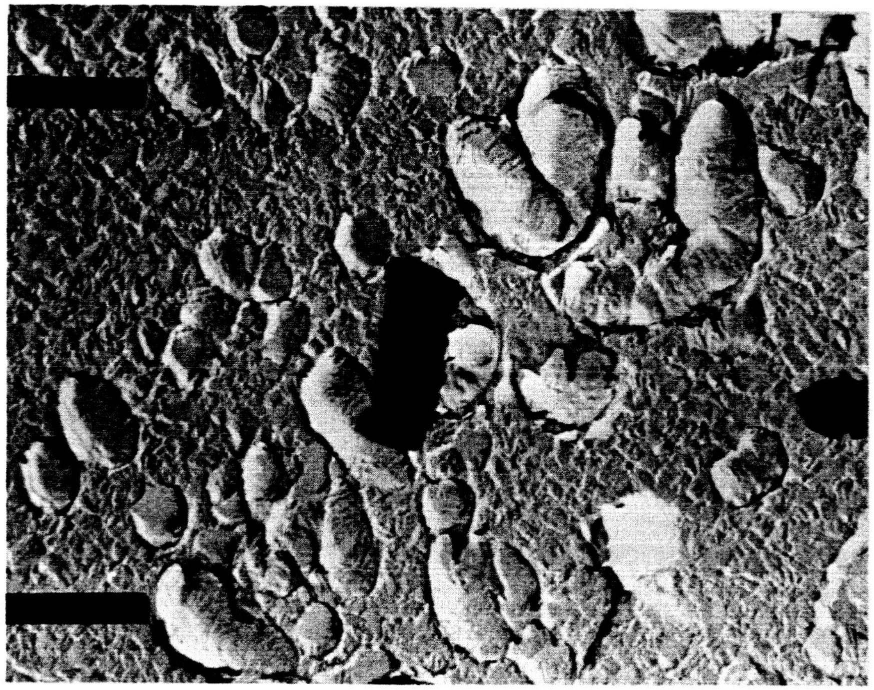
Electron Micrograph of Sample N-84.
GaAs Deposited on (111) Si at 400°C.
(Replica Made from the Underside of
the GaAs Film). Mark indicates 1μ.

Electron Micrograph of Sample N-88
GaAs Deposited on (111) Si at 500°C.
Mark Indicates 1μ.

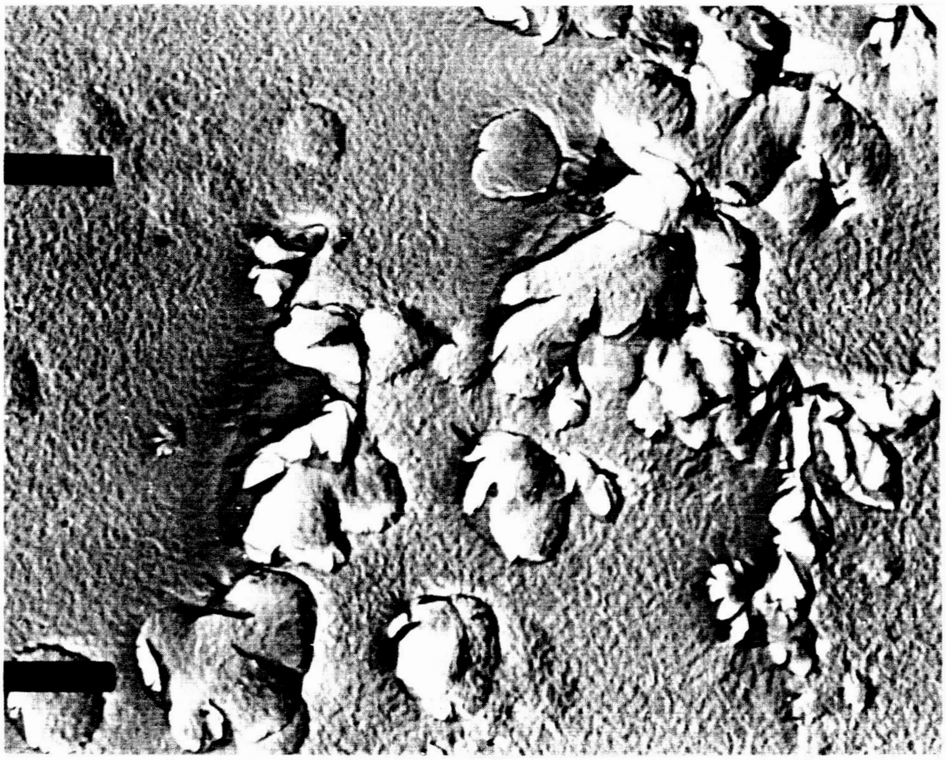
Figure 49



Electron Micrograph of Sample N-88
GaAs Deposited on (111) Si at 500°C.
Mark Indicates 0.5μ.



Electron Micrograph of Sample N-89.
GaAs Deposited on (111) Si at 550°C.
Mark Indicates 1μ.

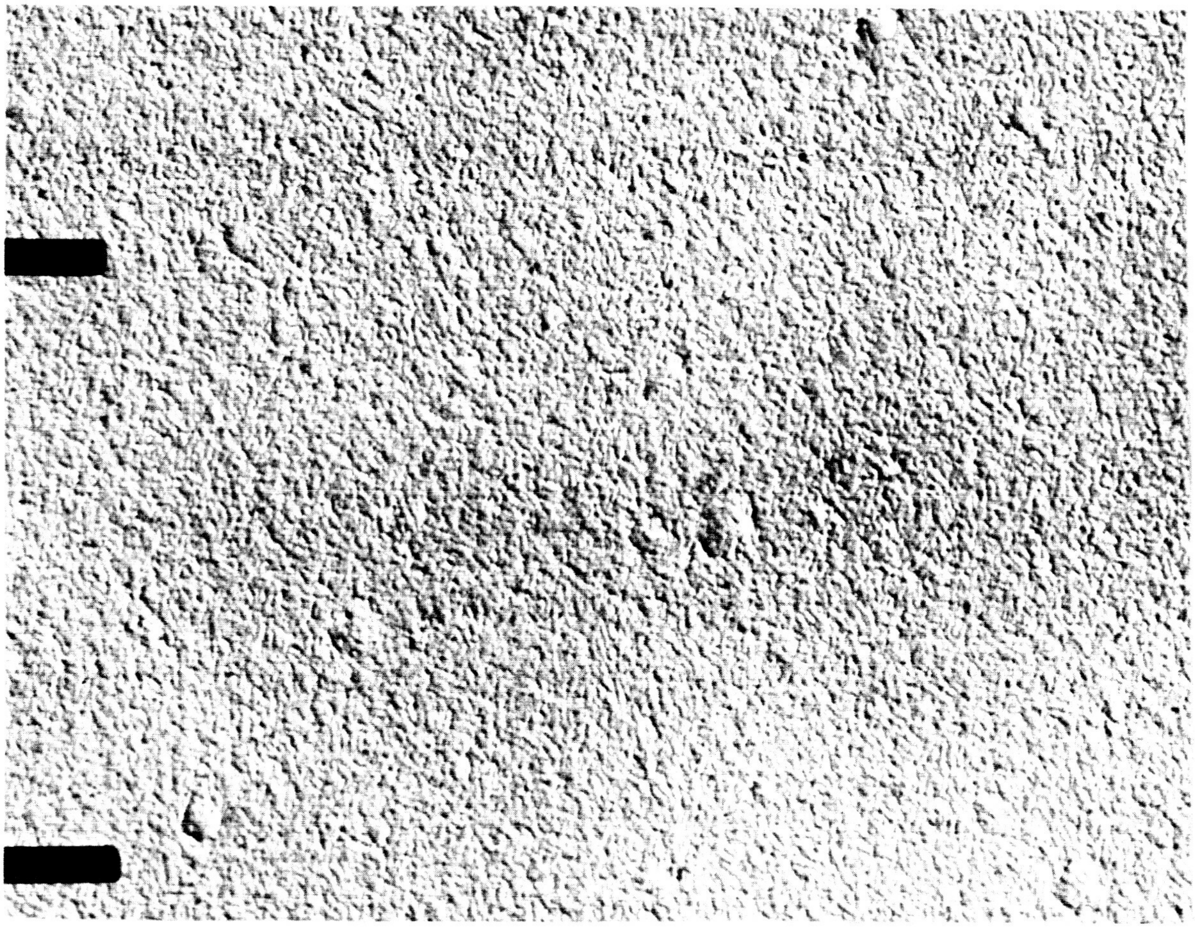


ELECTRON MICROGRAPH OF SAMPLE N77B.

GaAs FILM DEPOSITED ON (111) ORIENTED

Si AT 600° C.

MARK INDICATES 1μ.

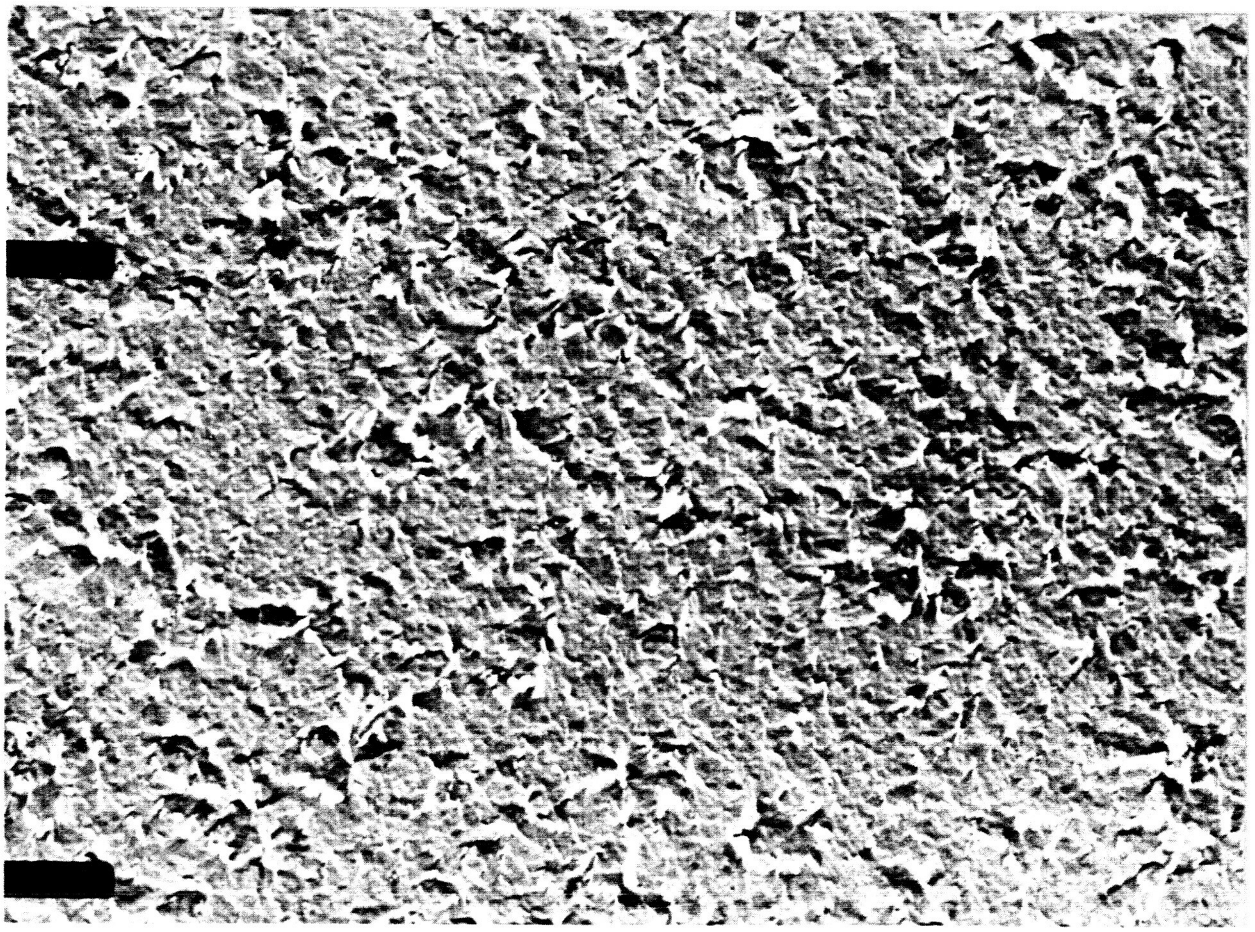


ELECTRON MICROGRAPH OF SAMPLE N144D.

GaAs FILM DEPOSITED ON (111) ORIENTED

Ge AT 500° C.

MARK INDICATES 1μ.



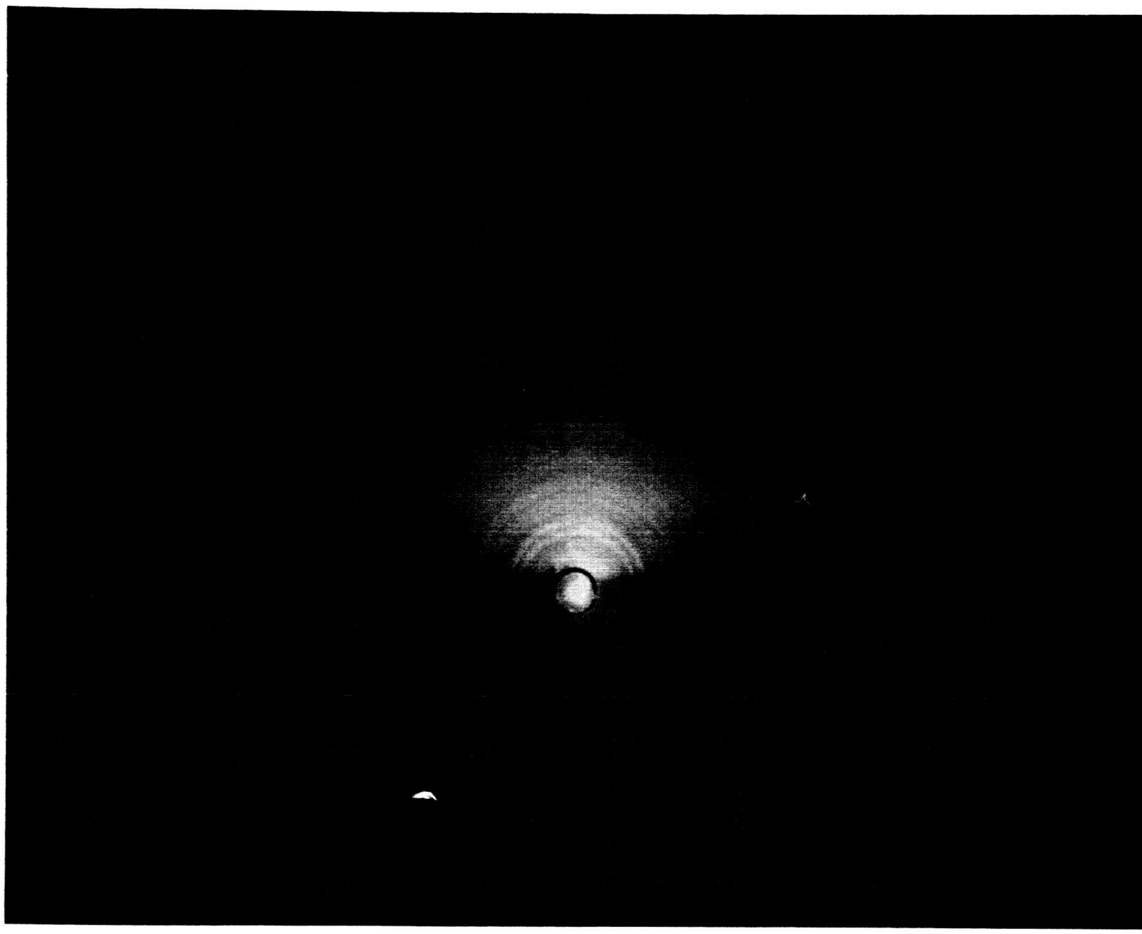
ELECTRON MICROGRAPH OF SAMPLE N144C.

GaAs FILM DEPOSITED ON GLASS (CORNING 7059)

AT 500° C.

MARK INDICATES 1μ.

Figure 54

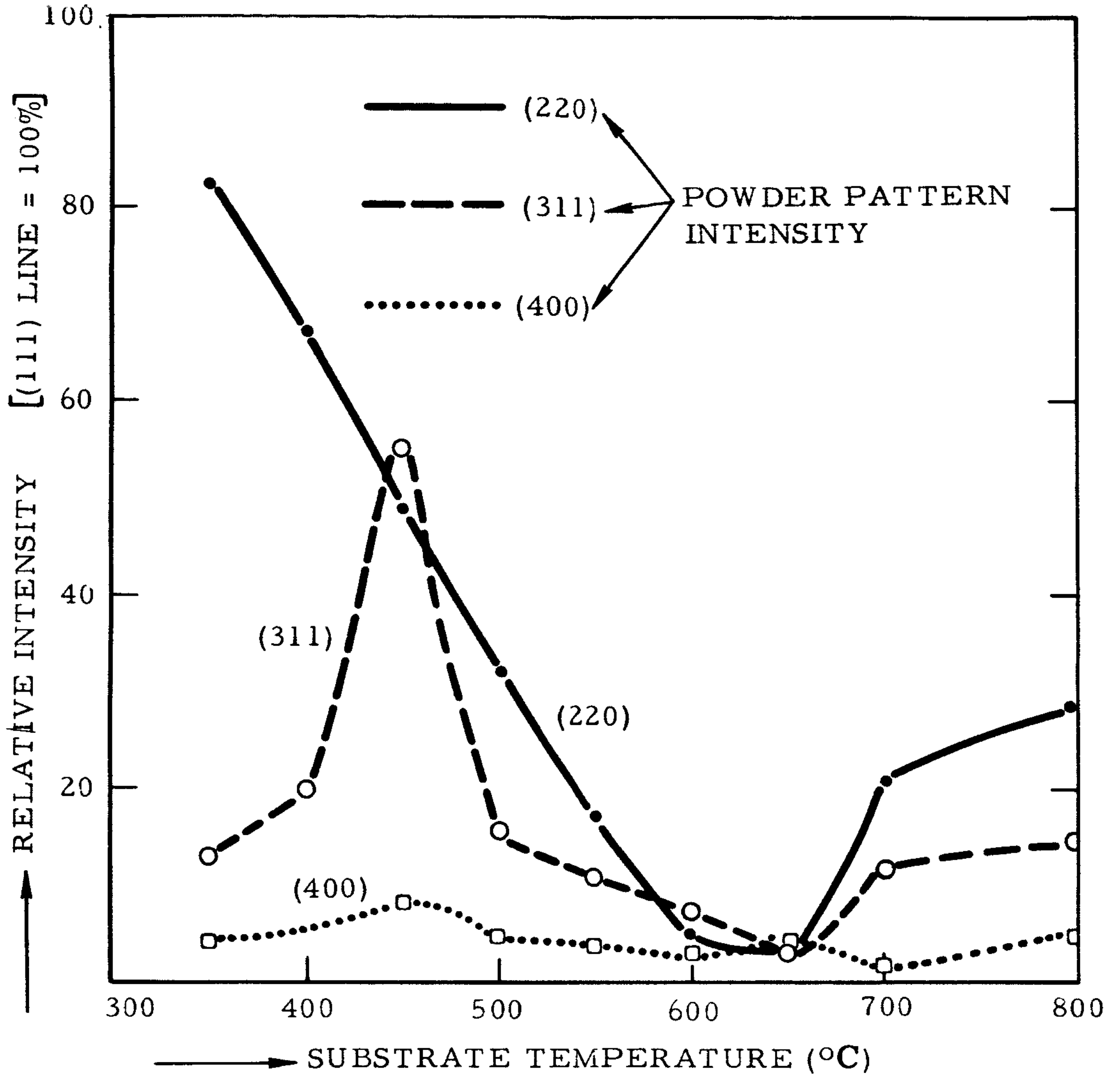


Electron Reflection Diffraction
Pattern of Sample N-89. GaAs
Film Deposited on (111) Oriented
Si at 550°C.

Figure 55

the variation of the crystallite size with different substrate temperatures by means of the electron reflection diffraction technique.

The structure of a number of GaAs films was investigated by x-ray diffraction techniques using a Norelco Geiger Müller counter wide-angle goniometer. The above-mentioned samples which were used in order to make replicas usually did not give a very satisfactory pattern when checked by x-ray diffraction. Although a (111) texturized pattern with an overlay of a powder pattern was obtained, the diffracted energy generally was too low to obtain conclusive results. The film thickness was only one micron or even less. In order to get a clearer picture of the influence of the substrate temperature upon the orientation of the GaAs films, a statistical evaluation was performed on 44 diffraction patterns of GaAs films. The samples were arranged into 9 groups according to the substrate temperature during the formation of the films, which ranged from 350 to 800°C. For each sample the relative intensity for the (220), (311), and (400) peak was determined in relation to the respective (111) peak. The relative intensities obtained were averaged for each group and plotted as a function of the substrate temperature. The graph is presented in Figure 56. The three curves have a minimum between substrate temperature of 600 to 700°C. In this temperature range all but a few of the GaAs crystallites are oriented such that the (111) plane is parallel to the substrate surface. This temperature range seems to be very favorable for the growth of GaAs films with a preferred orientation. At higher and, particularly, at lower temperatures then the 600 to 700°C range the relative intensity of the (220), (311), and (400) lines increase. This means that the orientation of the crystallites is more random and the x-ray diffraction pattern is similar to that of a GaAs powder. In the range investigated, between 350 and 800°C, the patterns always show a texturization but the relative intensities never reach the values of a powder pattern which are indicated as horizontal lines in Figure 56. The findings confirm somewhat the results obtained with the replica method. Higher substrate temperatures favor the formation of larger crystallites.



(220)
(311)
(400)
POWDER PATTERN INTENSITY
(311)
(220)
(400)
100
80
60
40
20
300
400
500
600
700
800
RELATIVE INTENSITY [(111) LINE = 100%]
SUBSTRATE TEMPERATURE (°C)

Figure 56

e) Electrical Measurements:

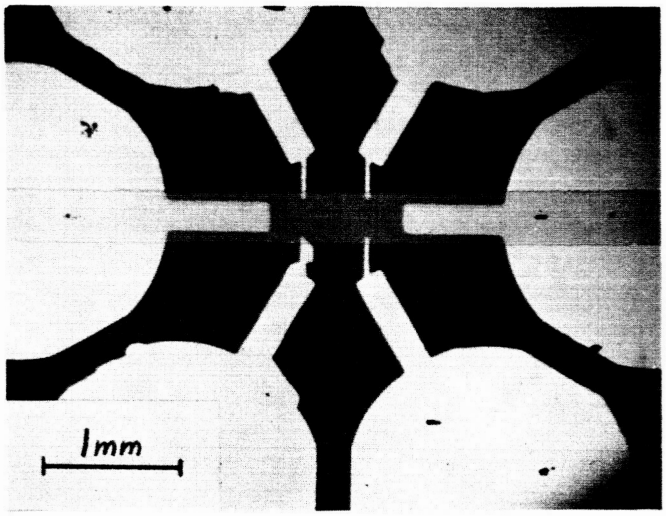
A masking arrangement was designed to fabricate samples for the measurement of the Hall-effect. An etched GaAs strip was provided with vacuum deposited tin-gold contacts and heat treated for about one minute at 350°C in hydrogen. A micrograph of a complete Hall sample is presented in Figure 57. The samples were placed in a Teflon-insulated holder with spring loaded points for the current and voltage contacts. By means of this pressure the substrate with the Hall-sample was held against a small graphite block. With this arrangement, substrate temperatures up to about 300°C can be applied. The substrate holder remained in a glass enclosure under vacuum for measurements at elevated temperatures.

The Hall-voltage was monitored with a General Radio Company d-c amplifier with an input impedance higher than $10^{13}\Omega$. The output of the amplifier was connected to a recorder. The amplifier was used also for the measurement of the sample current. For the determination of the voltage drop along the sample, a battery operated Keithly electrometer was used. A water cooled Varian electromagnet generated a magnetic field of 10,000 gauss in all experiments. The procedure for the evaluation of the data was taken from Pütley[41].

The results of the measurements of all investigated samples are summarized in Table II. Because of the high resistivity of the GaAs films, only good insulating materials like sapphire (α- Al_2O_3) or spinel ($MgO \cdot 3Al_2O_3$) were selected as substrates. The thickness of the GaAs layers was between 0.7 and 2.4μ.

As demonstrated in Table II, the values of the room temperature resistivity of the GaAs deposits scatter in a very wide range. Values as high as $3.3 \times 10^6 \Omega$cm and as low as $5.6 \times 10^3 \Omega$cm were obtained. In one instance, 30Ωcm was measured in a particular area of sample N-83A. However, this result was not reproducible. The room temperature resistivities of all samples are plotted as a function of the deposition temperature in Figure 58. This graph is not very conclusive, but it seems to indicate that, at higher substrates temperatures, higher resistivity values are more likely to occur.

The conductivity as a function of temperature is plotted in Figure 59 for several samples in the range between room temperature and about 300°C. In some cases



Micrograph of a Strip of GaAs with
Vacuum Deposited Gold Contacts
for Hall-effect Measurements.

Figure 57

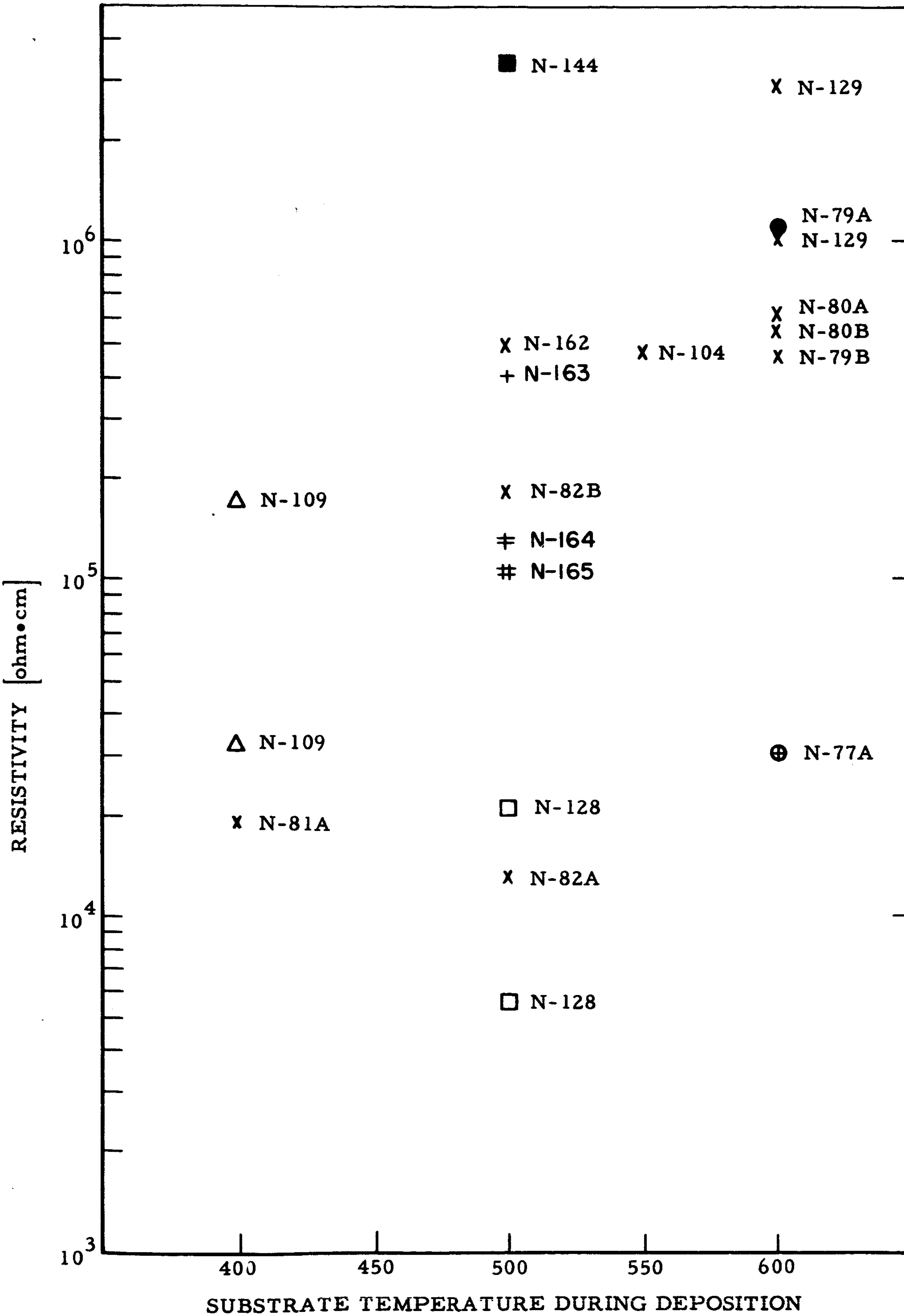
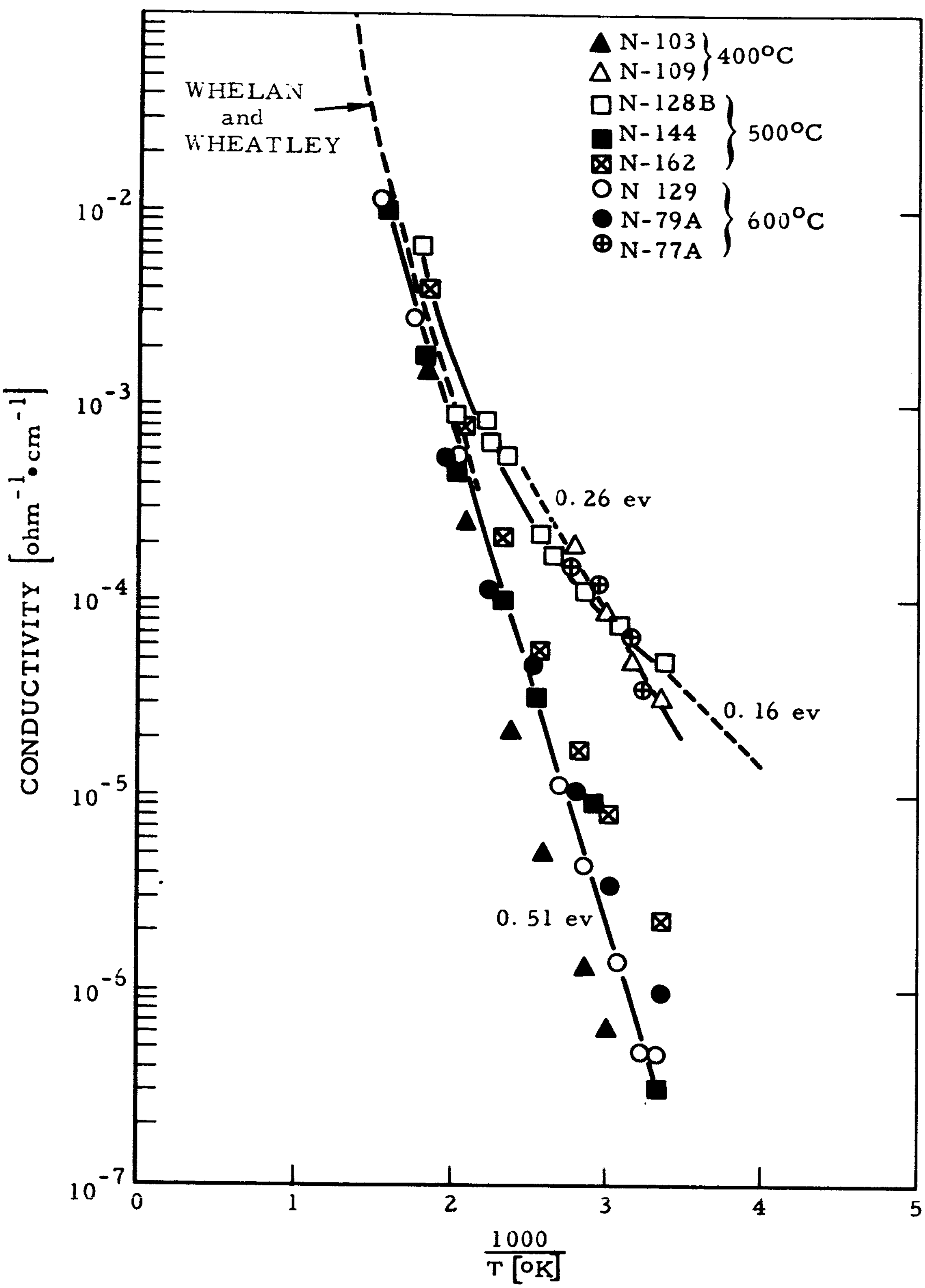

N-144
N-129
N-79A
N-129
N-80A
N-80B
N-79B
N-162
N-163
N-104
N-109
N-82B
N-164
N-165
N-109
N-77A
N-81A
N-128
N-82A
N-128
10^6
10^5
10^4
10^3
RESISTIVITY [ohm•cm]
400
450
500
550
600
SUBSTRATE TEMPERATURE DURING DEPOSITION

Figure 58



WHELAN and WHEATLEY
N-103
N-109
400°C
N-128B
N-144
N-162
500°C
N 129
N-79A
N-77A
600°C
0. 26 ev
0. 16 ev
0. 51 ev
CONDUCTIVITY [ohm⁻¹•cm⁻¹]
10⁻²
10⁻³
10⁻⁴
10⁻⁵
10⁻⁶
10⁻⁷
0
1
2
3
4
5
1000/T [°K]

Figure 59

Sample Number	Type of Substrate	Substrate Orientation	Substrate Temperature (°C)	Thickness of GaAs Layer (μ)	ρ at Room Temperature (ohm . cm)	Approx. Doping of Ga Source
N-77A	Sapphire	0° to c-axis	600		30,000	-
N-79A	Sapphire	0° to c-axis	600		1,070,000	-
N-79B	Sapphire	0° to c-axis	600	2.4	450,000	-
N-80A	Sapphire	0° to c-axis	600	1.5	600,000	-
N-80B	Sapphire	0° to c-axis	600	0.54	540,000	-
N-81A	Sapphire	0° to c-axis	400	0.07	19,000	-
N-82A	Sapphire	0° to c-axis	500	0.21	13,000	-
N-82B	Sapphire	0° to c-axis	500	0.15	180,000	-
N-83A	Sapphire	0° to c-axis	550	1.2	30	-
N-103	Spinel	(100)	400	0.3	7,500,000	-
N-104A	Sapphire	0° to c-axis	550	0.24	470,000	-
N-104B	Sapphire	0° to c-axis	550	0.18	350,000	-
N-109A	Spinel	(100)	400	1.0	32,000	-
N-109B	Sapphire	0° to c-axis	400	1.0	170,000	-
N-128A	Sapphire	90° to c-axis	500	1.2	5,600	0.003% Te
N-128B	Sapphire	0° to c-axis	500	1.2	21,000	0.003% Te
N-129A	Sapphire	0° to c-axis	600	1.8	2,800,000	0.003% Te
N-129B	Sapphire	0° to c-axis	600	1.2	> 1,000,000	0.003% Te
N-144	Sapphire	0° to c-axis	500	1.8	3,300,000	-
N-162	Sapphire	0° to c-axis	500	0.9	490,000	-
N-163	Spinel	(100)	500	0.75	420,000	0.05% Te
N-164	Sapphire	0° to c-axis	500	0.38	130,000	1% Te
N-165	Spinel	(100)	500	0.85	110,000	10% Te

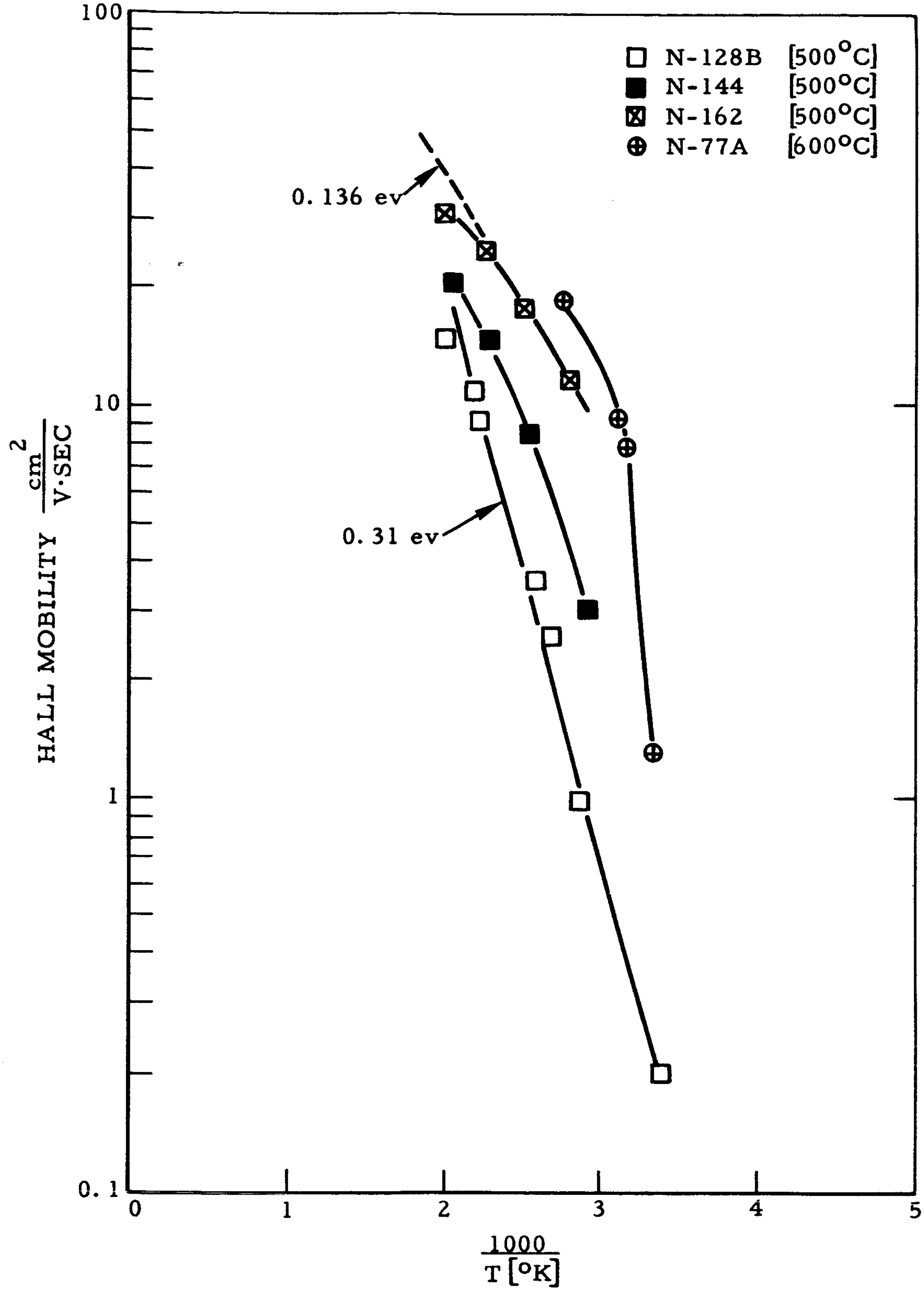
TABLE II

the conductivity increases about four orders of magnitude over the temperature range investigated. According to Figure 59, the samples apparently can be divided into two groups: One has a room temperature conductivity of 4×10^{-5} (ohm . cm)$^{-1}$ and an activation energy between 0.16 and 0.26 eV. The other has a conductivity which is almost 2 orders of magnitude lower and has an activation energy of 0.51 eV. So far, it was not possible to determine clearly a relation between the deposition parameters and the value of the conductivity or its activation energy. The 0.51 eV slope follows very closely the intrinsic conductivity for single crystal GaAs material as reported by Whelan and Wheatley[42]. Their conductivity values are shown in Figure 59 in a dashed line. It seems most likely, therefore, that the conductivity of the high resistivity GaAs films approaches the intrinsic conductivity of GaAs. The conductivity of the other samples with an activation energy of about 0.2 eV could be ascribed to impurity or defect levels. These samples apparently approach intrinsic conductivity also at the higher temperature range. However, the low mobilities measured indicate that a high degree of compensation probably exists.

An investigation of the Hall-effect was practically not possible at room temperature. The voltage across the Hall-contacts drifted and was very difficult to balance. In measurements on nearly all the undoped samples Hall-voltages have not been observed which could be interpreted unambiguously as above the noise level of the system. Considering the sensitivity of the apparatus, this means that the room temperature mobility is less than 1 cm^2/V sec.

The Hall-mobility could, however, be measured satisfactorily at higher temperatures. Figure 60 gives the relationship between temperature and mobility for four samples. The activation energy ranged from 0.136 to 0.31 eV. The highest mobility value obtained was 30 cm^2/V sec. at 210°C for the sample N-162 which was deposited at 500°C substrate temperature.

Figure 61 gives the carrier concentration between room temperature and approximately 340°C for several samples. The carrier concentration of the two undoped specimens increases from $10^{13} cm^{-3}$ to almost $10^{15} cm^{-3}$ with an activation energy of 0.46 eV.



N-128B [500°C]
N-144 [500°C]
N-162 [500°C]
N-77A [600°C]
0.136 ev
0.31 ev
HALL MOBILITY $\frac{cm^2}{V \cdot SEC}$
100
10
1
0.1
0
1
2
3
4
5
$\frac{1000}{T [^oK]}$

Figure 60

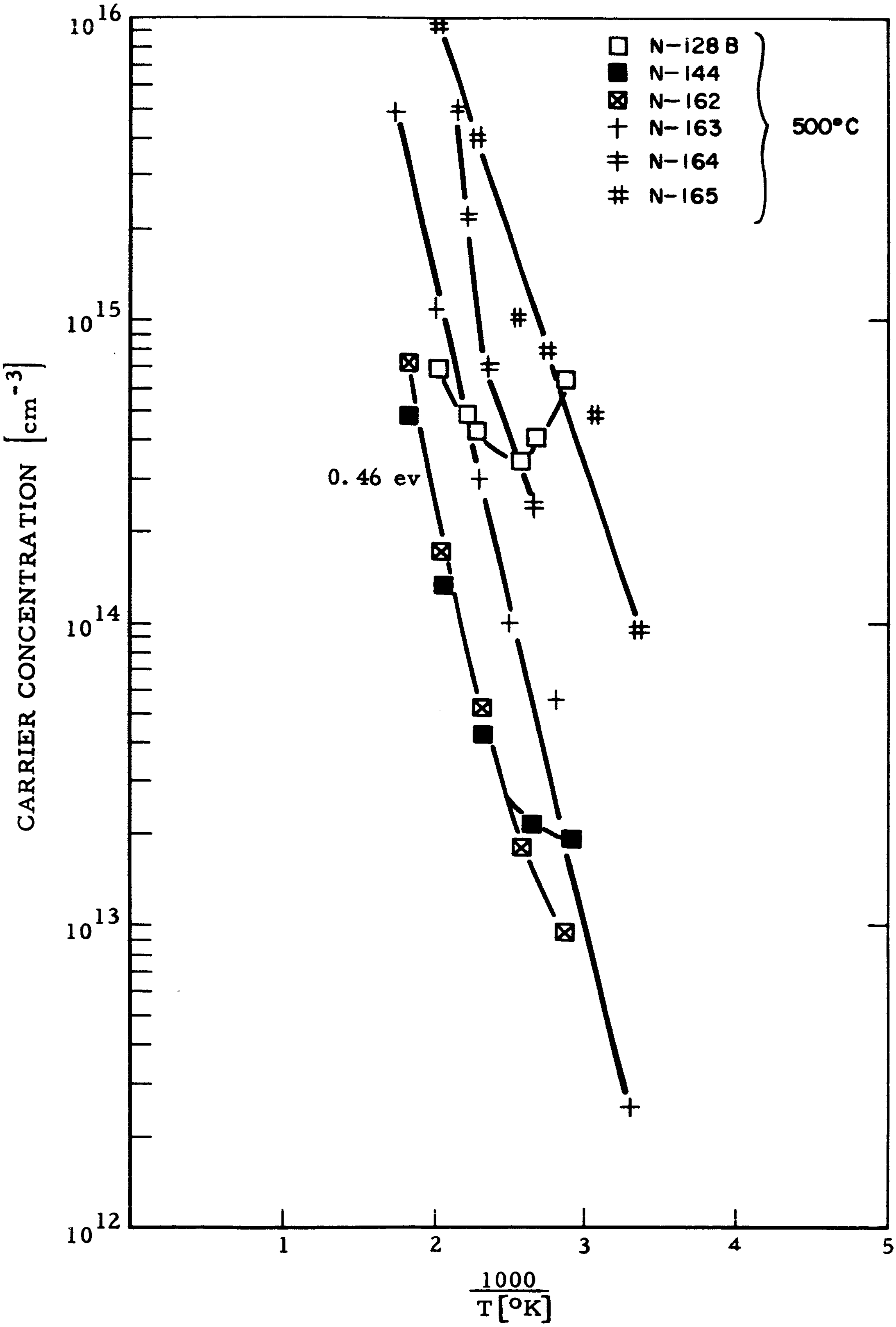

N-128 B
N-144
N-162
N-163
N-164
N-165
500°C
0.46 ev
CARRIER CONCENTRATION [cm^-3]
10^16
10^15
10^14
10^13
10^12
1
2
3
4
5
1000/T[°K]

Figure 61

Here again, as in the case of the determination of the mobility, it must be taken into consideration that the values at lower temperatures are not very accurate. Whenever a conclusive measurement of sufficient signal level was obtained, the sample was found to be of N-type conductivity regardless whether dopant was added or not.

f) Addition of Tellurium Dopant:

In 5 runs tellurium was added in a concentration range from 0.003 per cent to 10 per cent to the gallium before evaporation. Three GaAs films were analyzed by x-ray fluorescence technique and no tellurium was detectable. This means that the concentration was below 0.01 per cent. The surprisingly low concentration level of tellurium in the GaAs films most likely is a consequence of the high vapor pressure of this element. At 1000°C the difference in vapor pressure between gallium and tellurium is 6 orders of magnitude[40], as illustrated in Figure 44. Hence, in heating up the gallium tellurium mixture to 1000°C, most of the tellurium is evaporated onto the closed shutter before the deposition of GaAs is started. For the formation of GaAs films with a controlled concentration of a high volatile element, therefore, an additional crucible, containing the dopant only, would be advantageous. Such an arrangement would comprise a four temperature method.

The electrical measurements of tellurium doped GaAs samples were not conclusive. The conductivity and its temperature dependence was found to be similar to that of undoped GaAs. Hall mobility and carrier concentration values had a high degree of uncertainity because of the noise level of the Hall voltage. A higher carrier concentration of several tellurium doped samples is discernible from the measurements presented in Figure 61. Conductivity values were very similar to those of undoped samples.

3) Silicon-on-Sapphire by Heteroepitaxial Growth

a) Literature Survey:

The following is a selection and discussion of articles dealing with the hetero-epitaxial growth of silicon on foreign substrates. The growth of silicon layers on substrates by means of gaseous silicon compounds has been under investigation for several years. The compounds are either reduced in hydrogen or they are thermally decomposed to obtain the elemental silicon.

Epitaxial deposition of silicon on single crystal quartz substrates was performed in 1963 by Joyce, Bicknell, Charig, and Stirland[43] with the hydrogen reduction of $SiHCl_3$. Rasmanis[44] grew silicon films on glazed polycrystalline Al_2O_3 substrates with the hydrogen reduction of $SiCl_4$. This method was called "rheotaxy" because the glaze is molten at the deposition temperature. Growth of silicon layers on sapphire substrates was reported[45] in 1963 and first published in 1964 by Manasevit and Simpson[46] who again employed the hydrogen reduction of $SiCl_4$. Their initial results were obtained on substrates produced by cutting a sapphire rod perpendicular to its fastest growth direction which is approximately 60° from the c-axis. Large single crystal areas of silicon were reported.

Mueller and Robinson[47] used the pyrolythic decomposition of SiH_4 to grow silicon films on single crystal sapphire. Doo[48] deposited silicon on poly-crystalline Al_2O_3 with the $SiCl_4$ process. After melting and regrowth large grain silicon films were obtained. The resistivities had values between 0.05 and 0.1 Ωcm for layers on high purity substrates. Bicknell, Charig, Joyce, and Stirland[49] presented a study of the morphology of silicon films on single crystal quartz. Their experiments were carried out with $SiHCl_4$.

A detailed study concerning primarily the deposition parameters and the epitaxial relationship between the silicon deposit and various sapphire orientations was presented in 1965 by Manasevit, Miller, Morritz, and Nolder[50] and by Nolder and Cadoff[51]. Joyce, Bennett, Bicknell and Etter[52] investigated silicon films on single crystal substrates of quartz and Al_2O_3 employing the hydrogen reduction of $SiHCl_3$ and the pyrolysis of SiH_4. Porter and Wolfson[53] used

$SiCl_4$, $SiHCl_3$, and $SiBr_4$ as well as SiH_4 for silicon deposition on single crystal aluminum oxide and they discussed the usefulness of these compounds for epitaxial growth.

(100) and (111) oriented single crystal spinel wafers were used by Seiter and Zaminer[54] for epitaxial growth of silicon with the $SiCl_4$ process.

The occurrence of twinning in silicon layers on sapphire substrates was investigated by Nolder, Klein, and Forbes[55]. Stresses which are developed in a silicon layer on sapphire due to the mismatch in thermal expansion coefficients can deform the substrate. This was pointed out by Dumin[56].

A study of the epitaxial relationship of silicon layers on commercially available magnesium aluminate spinel was presented by Manasevit and Forbes[57]. The deposits were grown with $SiCl_4$ and SiH_4. Dumin and Robinson[58] investigated the doping of silicon layers caused by diffusion of aluminum ions from the sapphire substrate during growth or annealing of the film. The epitaxial growth of silicon on silicon carbide substrates by the decomposition of SiH_4 was studied by Tallman, Chu, Gruber, Oberly, and Wolley[59].

b) The $SiCl_4$ Process:

The initial experiments for the deposition of silicon on sapphire were carried out in the Hughes Solid State Research Center by reduction of $SiCl_4$ with hydrogen. The furnace as well as the experimental parameters were exactly the same as for the growth of silicon on silicon:

1) SiC covered graphite boat in a 3 inch I.D. horizontal tube.
2) Deposition temperature 1125° (indicated).
3) Hydrogen flow rate (carrier gas) 26,000 cm^3 per minute.
4) Flow rate of hydrogen saturated at room temperature with $SiCl_4$ 220 cm^3 per minute.
5) Growth rate 0.3μ per minute.

The sapphire substrate wafers, obtained from several commercial sources, were of 0°, 60°, and 90° orientation with respect to the c-axis.

Figure 62 is a photomicrograph of a silicon deposit on a 0° oriented sapphire wafer made with the $SiCl_4$ process at 1150°C. The habit of the growth shown in this picture can be considered typical for the result of a large number of runs made with similar parameters. Silicon crystals up to about 20μ in diameter are scattered randomly on the sapphire surface. Between the crystals exist areas where no silicon is deposited at all. Figure 63 shows the same section as Figure 62, with the difference that the substrate was brought into focus. Etching of the substrate takes place in those areas where no silicon is deposited.

Cross section of silicon deposits on sapphire substrates are illustrated in Figure 64. A film in the initial stage of growth corresponding to the photographs in Figure 62 and 63, is shown in Figure 64a. With prolonged deposition time, it is sometimes possible to cover the entire substrate with a film whose structure is shown in Figure 64b. In spite of the unoriented growth, this type of deposit permits the construction of good quality MOS-devices after the layer is polished down to 1 or 2μ. Because of the large size of the crystals, the devices can, in principle, perform similar to those on a single layer of crystal silicon. However, a film like that in Figure 64b is the exception rather than the rule with the $SiCl_4$ process. What normally happens is that the holes in the silicon layer cannot be closed; not even with prolonged reaction time. If the specimen is left longer in the reactor than the period which would normally give a 5 to 10μ growth at a certain set of experimental parameters, the substrate is gradually etched in all the areas where no silicon was initially deposited. The photomicrograph in Figure 63 is focused on the etched surface. Figure 64c shows the cross section of a film with etch pits.

The severe etching in certain areas of the sapphire surface apparently is attributed to the attack by chlorine and HCl which are the reaction products of the reduction of $SiCl_4$ with hydrogen. The occurence of such an etching reaction is suggested by the improvement in the quality of the silicon layer with decreasing deposition temperature and increasing concentration of the $SiCl_4$ vapor (i.e., increasing deposition rate). This behavior is contrary to the fact that lower temperatures and high supersaturation ratios increase the nucleation rate and reduce the mobility of the absorbed atoms on the substrate surface, both of which promote polycrystallinity. The deterioration of the substrate surface is most severe at high temperatures. Furthermore, the quality of the silicon layer improves markedly if a low temperature "flash" deposition preceeds the high temperature deposition cycle. Conversely, as it was pointed out by Porter and Wolfson[53], the quality of the silicon layers is abruptly lowered by the introduction of HCl vapor into the hydrogen stream with the silicon compound. According to these authors, the use of $SiHCl_3$ seemed to improve the silicon films, particularly at lower temperatures. $SiBr_4$, on the other hand, gave results similar to $SiCl_4$.

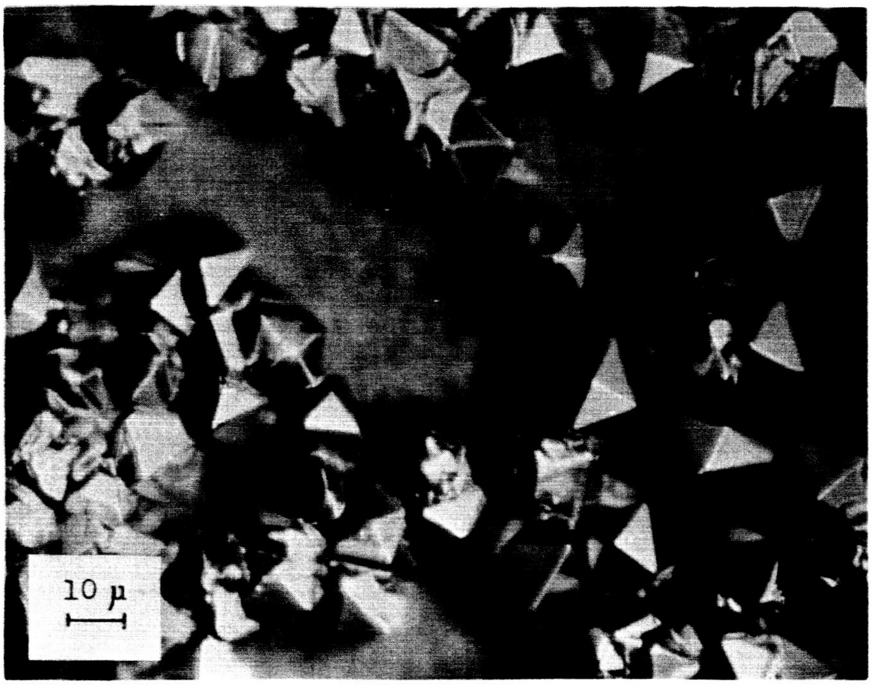
Silicon depositions at lower temperatures, e.g. between 950° and 1050°, resulted in films which had a smoother surface and a lower number of holes. In spite of the apparent perfection of these films, they were electrically of low quality. The films had high resistivities and low mobilities.

Figure 65 is an x-ray diffraction recording of a silicon film on an 0° oriented sapphire substrate deposited with $SiCl_4$ at 1100°C. The α-Al_2O_3 lines (006) and (0.0.12) appear together with a silicon pattern which is indicative of randomly oriented grains slightly texturized in the (111) direction. Although occasionally better oriented films were obtained, the presented pattern can be considered as being typical of the majority of layers grown under similar conditions.

The quality of the films apparently is governed strongly by the number of silicon nuclei formed in the very beginning of the deposition process. Whenever the surface can be densely covered with silicon nuclei, a coherent film may eventually be formed during the reaction period. But if there are initially only a few places on the substrate where a nucleation took place, the etching of the substrate in the silicon free areas will prevent any further nucleation and hence a low quality deposit is formed. Because of the very poor reproducibility of the $SiCl_4$ process, any study of the nucleation phenomena would require a statistical evaluation. In view of the better results with SiH_4, as described in the following chapter, no further investigation was made with $SiCl_4$.

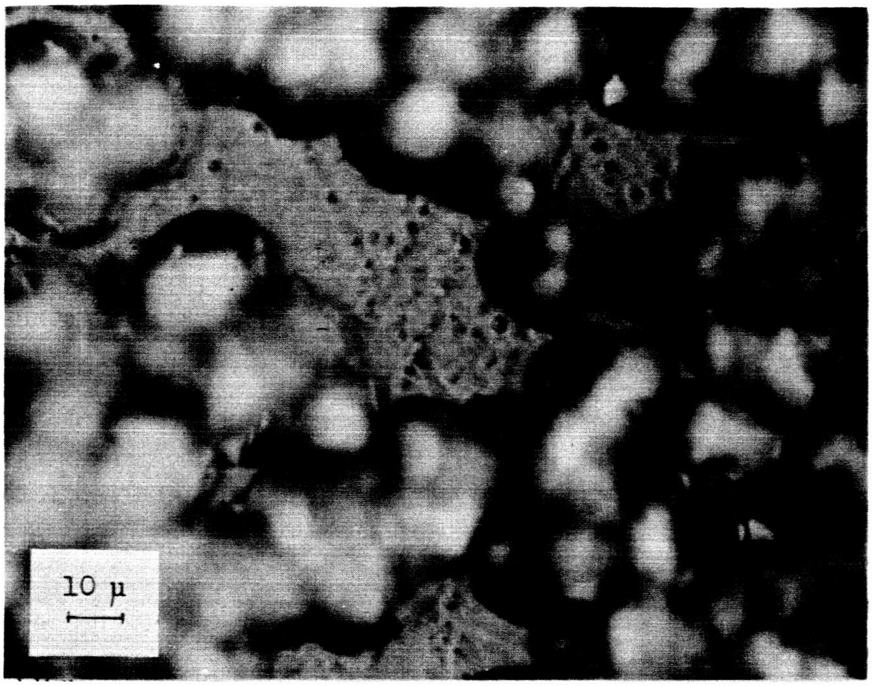
c) The SiH_4 Process:

The silicon depositions were performed in a vertical quartz reactor tube with about 7.5 cm I.D. After cleaning in boiling HCl and in an ultrasonic bath with



Photomicrograph of Sample S-187. The Focus is on the Silicon Crystals which are Randomly Deposited on the Sapphire Substrate Wafer. $SiCl_4$ Process.

Figure 62



Photomicrograph of Sample S-187. (Same area as Previous Picture) The Focus is on Etch Pits on the Sapphire Surface in one of those areas where Silicon did not Deposit.

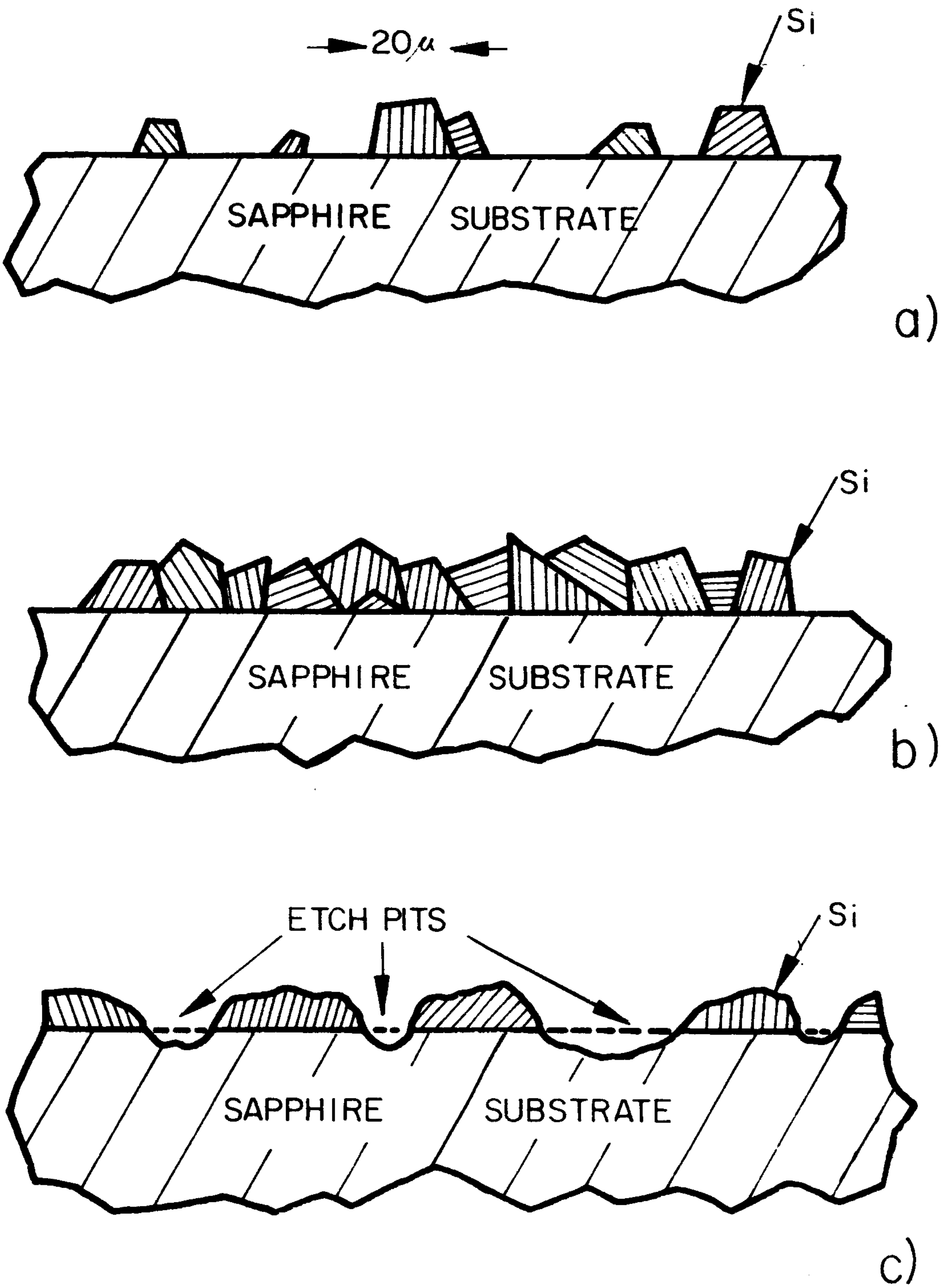

20μ
Si
SAPPHIRE SUBSTRATE
a)
Si
SAPPHIRE SUBSTRATE
b)
ETCH PITS
Si
SAPPHIRE SUBSTRATE
c)

Figure 64

alcohol or TCE, the sapphire specimens were placed on a SiC covered carbon pedestal which was RF heated from a coil around the reactor tube. The flow rates in most of the runs were 15 cm^3/min. of SiH_4 and 20,000 cm^3/min. of hydrogen at atmospheric pressure. A typical run was made at an indicated temperature of 980°C for 60 minutes which resulted in a 5μ thick layer. For most of the runs, $(\bar{1}012)$ oriented substrate wafers were used as suggested by Manasevit et. al.[50].

The silicon layers obtained by means of the SiH_4 process showed a considerable improvement in comparison with those made with $SiCl_4$. The films were dense, and very often they were shiny with a mirror like surface. This indicates that the first silicon atoms were densely and homogeneously nucleated over the whole surface. An x-ray diffraction recording which can be considered typical for many silicon films on sapphire substrates with the $(\bar{1}012)$ orientation is presented in Figure 66. Besides the (102), (204), and (306) peaks of α-Al_2O_3, there is a very strong (400) and a weak (111) peak of silicon. The (220) reflection of silicon coincides with the CuK_β peak of (204) α-Al_2O_3 which could not be suppressed even with a Ni-filter. The pattern indicates the silicon film to be of a strongly preferred orientation. Evidently this pattern demonstrates a considerably higher film quality than the pattern in the previous Figure 65.

The recording presented in Figure 66 is typical for many of the silicon deposits investigated. Other orientation of the sapphire besides the $(\bar{1}012)$ generally yielded a less pronounced texturization of the silicon film.

Figure 67 is photomicrograph of a silicon film on a $(\bar{1}012)$ oriented sapphire substrate. The film was photographed as deposited and no chemical etch was applied. The surface of this silicon layer is comparatively smooth considering the high magnification which was 760x. Many grains have a four fold symmetry and they seem to be oriented with respect to each other. The photograph suggests the (100) growth direction to be predominate.

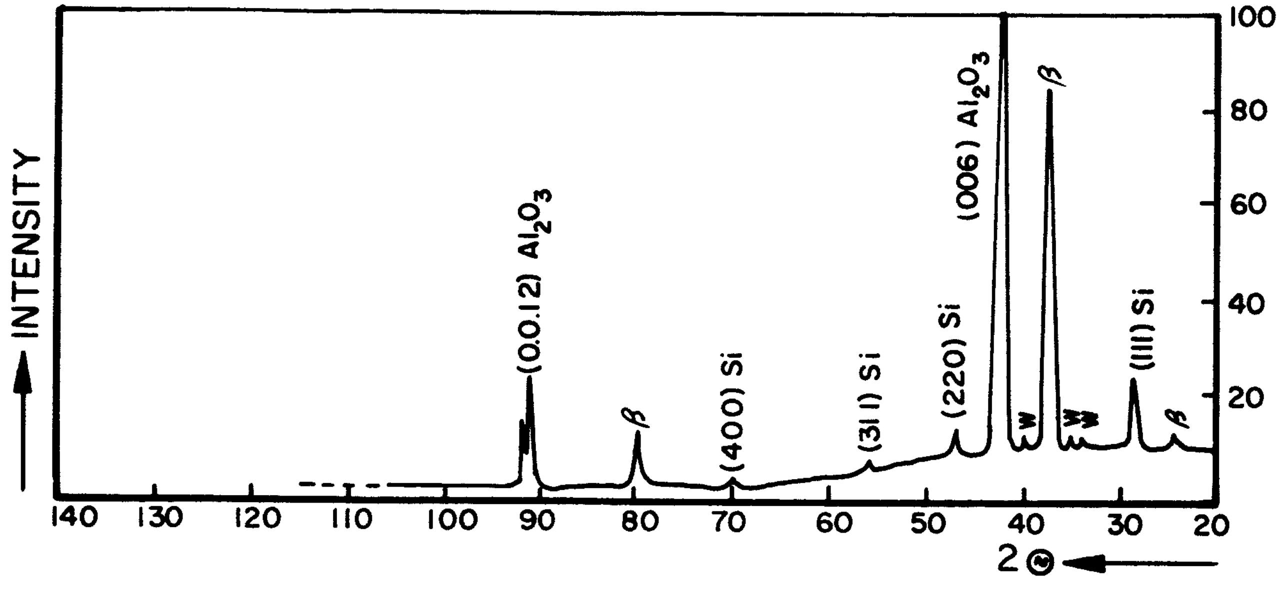


Figure 65

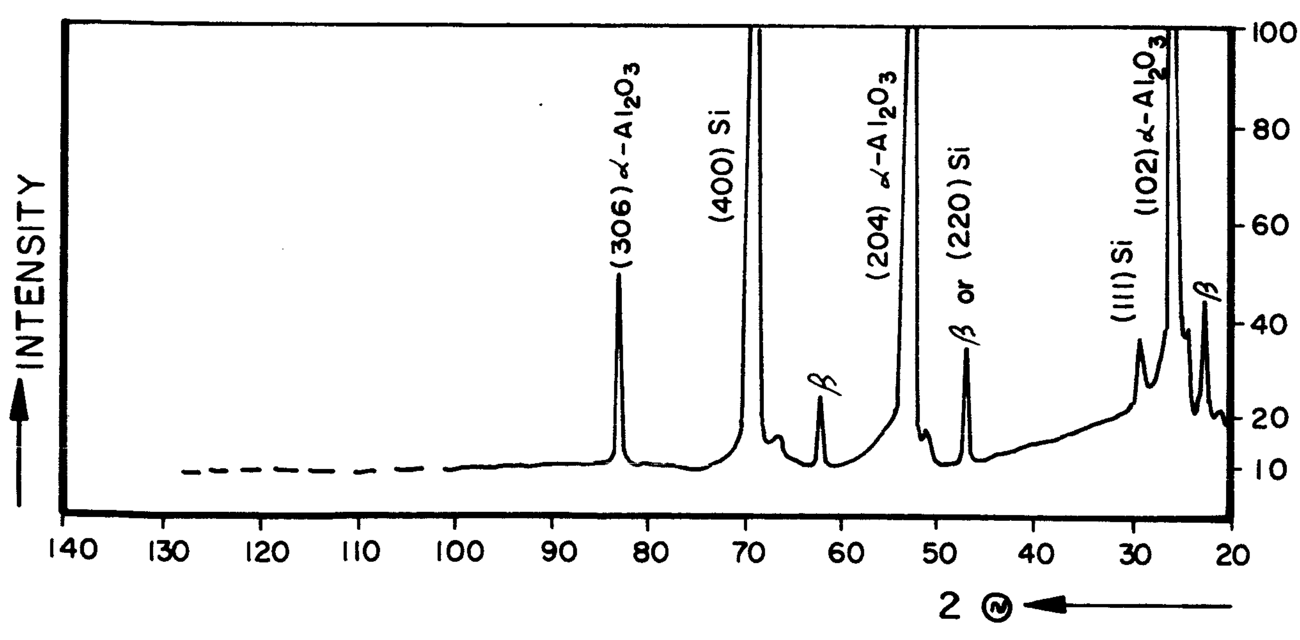
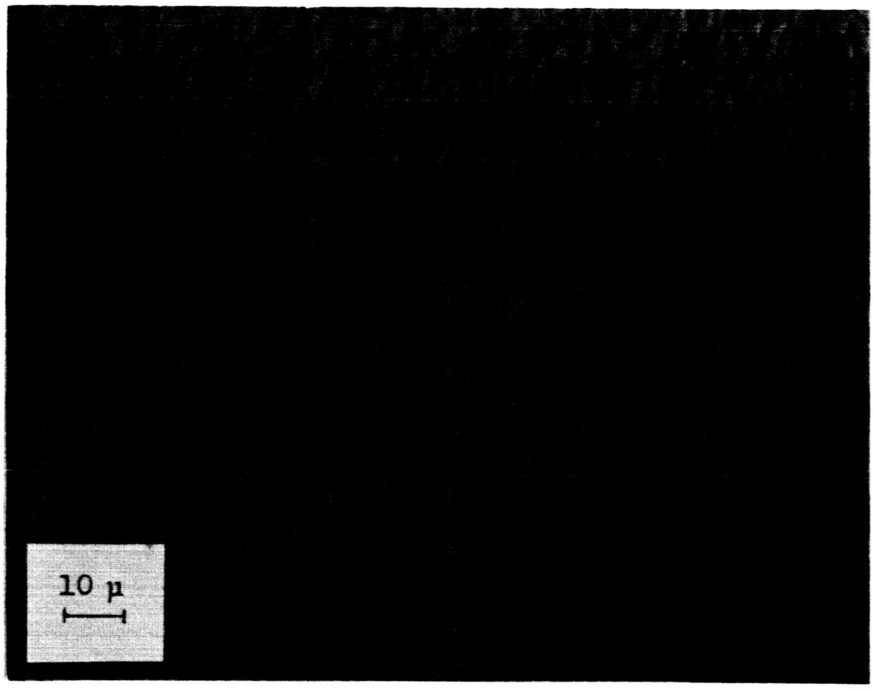


Figure 66

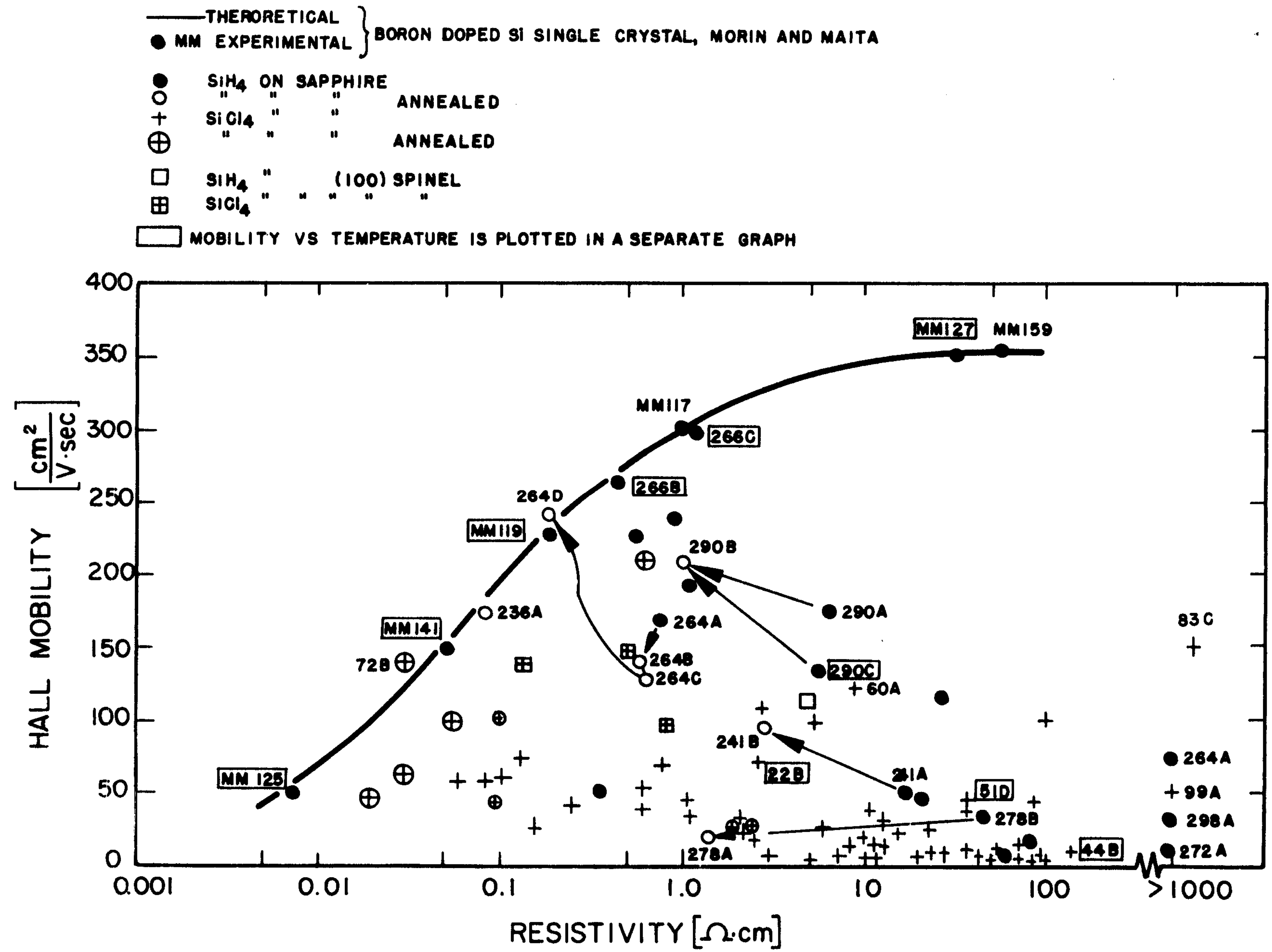


Photomicrograph of Sample S-329A. Silicon Thin-Film on a ($\bar{1}012$) Oriented Sapphire Substrate with Indication of a Four-Fold Symmetry.

d) Electrical Measurement:

The electrical properties of a great number of silicon films were investigated in order to obtain a quality measure of the deposited material. A 250μ wide silicon strip was etched out and provided with evaporated and alloyed aluminum contacts. The prepared silicon strip had the same geometry as the GaAs specimen in Figure 57. All silicon samples turned out to be of P-type conductivity. The Hall mobility is plotted as a function of the resistivity in Figure 68 for silicon layers grown on sapphire of various crystallographic orientations and on (100) oriented spinel employing both the $SiCl_4$ and the SiH_4 process. For comparison, experimental points are shown for boron doped single crystal silicon and a theoretical curve, both taken from Morin and Maita[60]. Some specimens were measured as deposited, others subjected to heat treatments up to 10 hours at temperatures around 1150°C. Figure 68 shows that the mobility of the samples investigated has a distribution from very low values to those of single crystal material. The graph clearly indicates the superiority of the SiH_4 process since the samples with the lower values of mobility are made mostly with $SiCl_4$. The arrows in Figure 68 refer to heat treatments. Any annealing decreases the resistivity and increases the carrier concentration and it generally improves the hole mobility of the samples. The increasing in doping concentration is also always observed with higher pedestal temperature during the growth of the film. The annealing cycles cause aluminum to diffuse from the substrate into the silicon layer[58].

The Hall mobility of 4 single crystal silicon samples and of 6 silicon on sapphire samples is plotted versus temperature in Figure 69. Above 300°C the mobilities of the high quality films approach the values of single crystal material and follow the well established temperature relation of $\mu \sim T^{-5/2}$. The effect of the defect structure of the silicon films grown on sapphire is very pronounced at the temperatures where impurity scattering normally dominates the lattice scattering. An average defect density can be estimated by comparing sample 266B with specimen MM141 and MM119 in Figure 69. Although sample 266B has a carrier concentration of about $5 \times 10^{16} cm^{-2}$ at room temperature, it behaves like a material doped with a concentration between $10^{17} cm^{-3}$ and $10^{18} cm^{-3}$. It is therefore estimated, that the defect density is around $5 \times 10^{17} cm^{-3}$,



THERORETICAL
MM EXPERIMENTAL
BORON DOPED Si SINGLE CRYSTAL, MORIN AND MAITA
SiH4 ON SAPPHIRE
" " " ANNEALED
SiCl4 " "
" " " ANNEALED
SiH4 " (100) SPINEL
SiCl4 " " " " "
MOBILITY VS TEMPERATURE IS PLOTTED IN A SEPARATE GRAPH
HALL MOBILITY [cm²/V·sec]
RESISTIVITY [Ω·cm]
400
350
300
250
200
150
100
50
0
0.001
0.01
0.1
1.0
10
100
>1000
MM127
MM159
MM117
266C
266B
264D
MM119
290B
290A
236A
264A
MM141
72B
264B
264C
290C
60A
83C
241B
22B
21A
51D
278B
278A
44B
264A
99A
298A
272A
MM 125

Figure 68

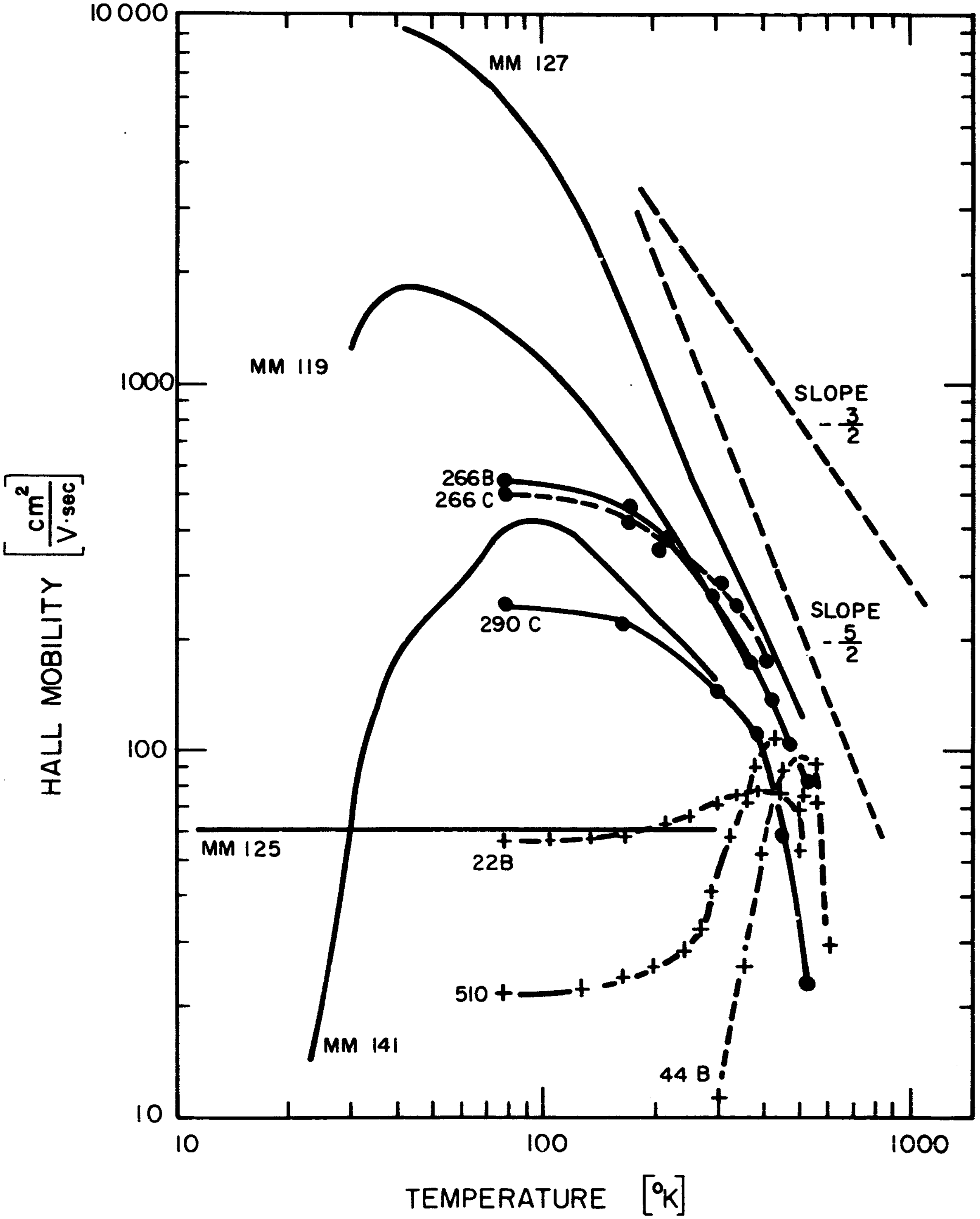

10 000
1000
100
10
10
100
1000
HALL MOBILITY $\left[\frac{cm^2}{V \cdot sec}\right]$
TEMPERATURE [°K]
MM 127
MM 119
SLOPE $-\frac{3}{2}$
SLOPE $-\frac{5}{2}$
266B
266 C
290 C
MM 125
22B
510
MM 141
44 B

Figure 69

and the mobility below about 200°K is mainly determined by defect center scattering. The electrical parameters of all the samples presented in Figure 69 are summarized in Table III for comparison.

e) Silicon Film Structure:

The diffractometer recording, shown in Figure 66, reveals a pattern very similar to that of a single crystal material. The electrical measurements however, presented in Figure 68 and 69 and in Table III do suggest, that the silicon films are not of true single crystal nature and incorporate a certain defect structure. The lowering of the Hall mobility below the value of single crystal material of equivalent impurity concentration, is caused by these defect centers. To clarify the morphology of the films, several samples were investigated with the electron microscope by reflection diffraction techniques. This evaluation indicated that good films do consist of large single crystal areas. Figure 70 is an example of the results obtained with the electron microscope. Figure 71 indicates twinning in the grown film which is observed quite frequently.

The structure of these heteroepitaxial films can be easily understood by examining Figure 72. This figure shows a hypothetical system of the substrate-to-film interface, where four atoms of the substrate correspond to three atoms of the layer. We assume that two nuclei were formed initially, one at the left and one at the right side of the picture. As the nuclei grow, an oriented film is formed on the substrate. A lattice mismatch is generated at the interface, where the crystallites join due to the lateral growth. When the structure of a silicon layer on a $(\bar{1}012)$ oriented sapphire wafer is constructed it might look like the sketch in Figure 73. The (001) direction of the silicon areas are all oriented parallel and perpendicular to the surface. The (100) directions are parallel as well. Between the single crystalline areas are the enlarged translation boundaries. It should be noted that such a film has a much higher degree of preferred orientation than, for example, a CdS film on a flat substrate where the c-axis of all crystallites are parallel, but the a-axis are randomly oriented. The translation boundary presents a severe distortion of the lattice and this

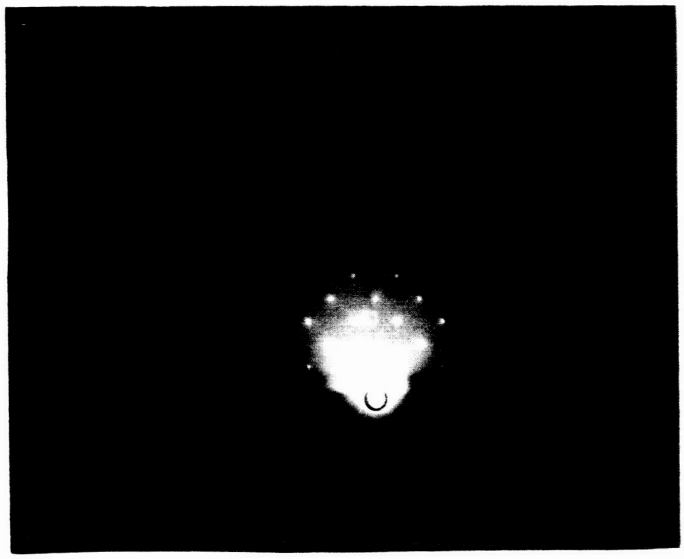


Figure 70

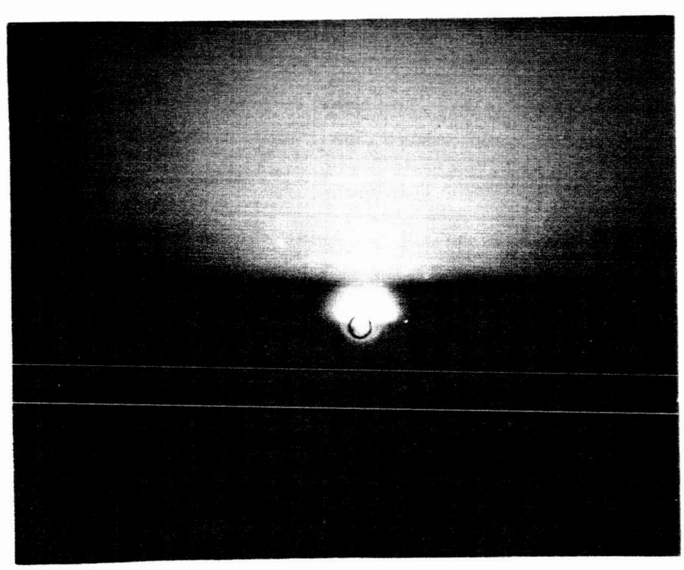


Figure 71

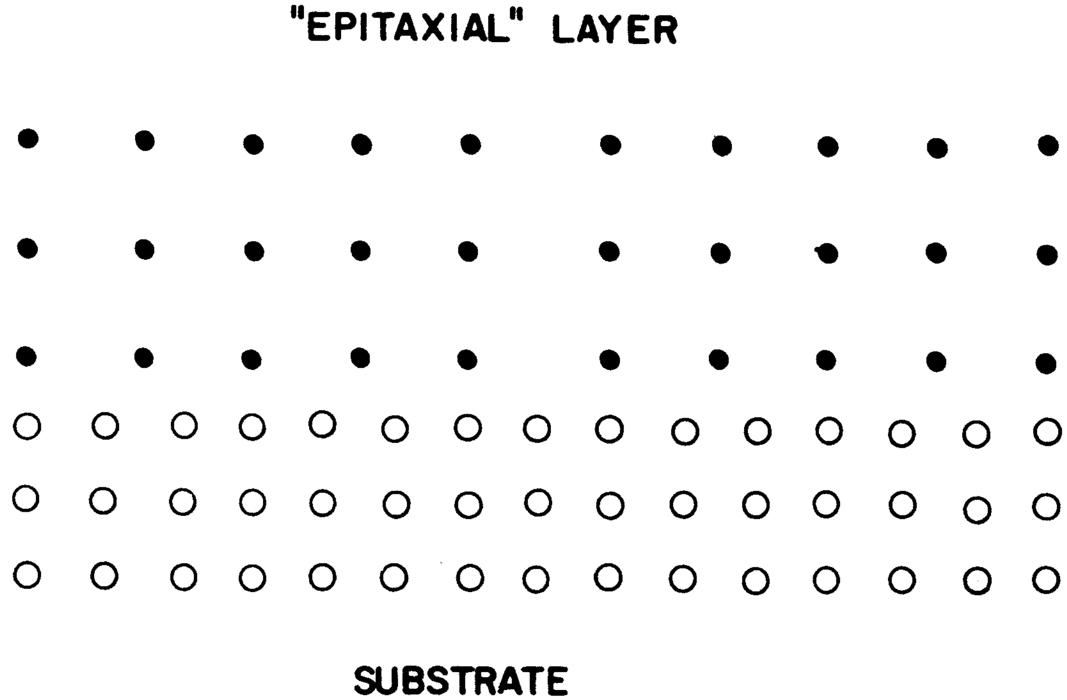


Figure 72

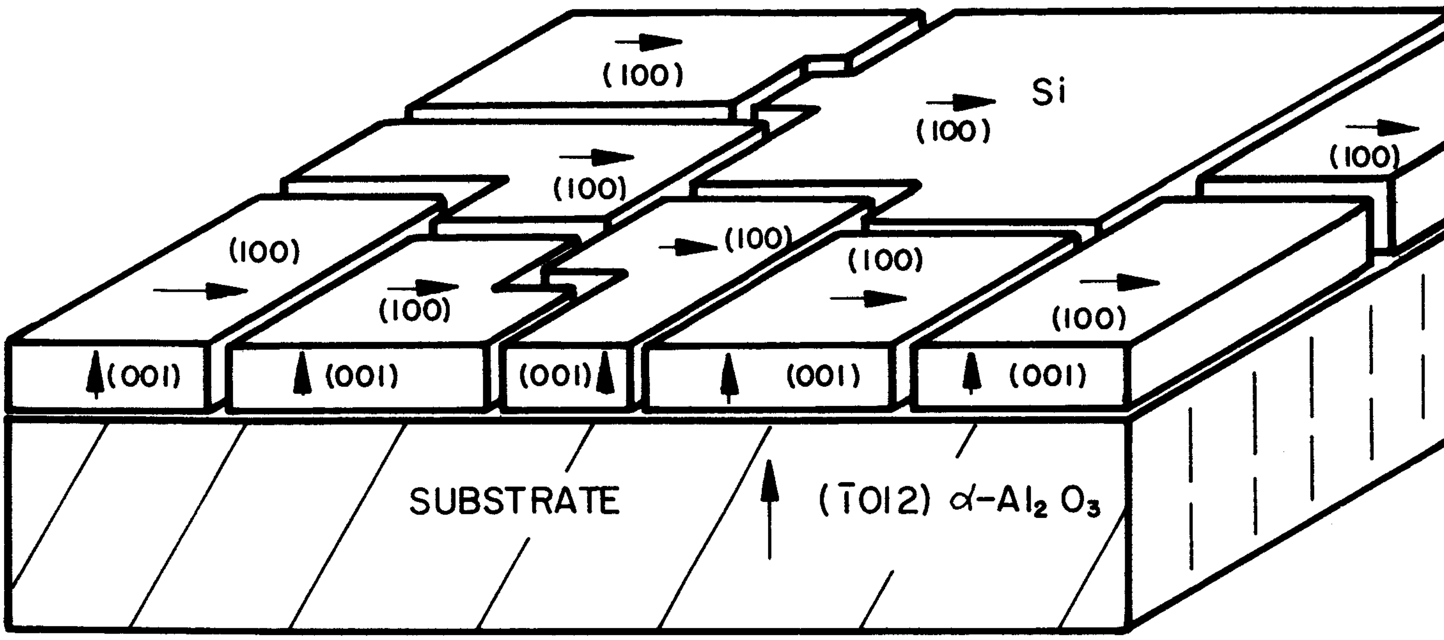

(100)
Si
(100)
(100)
(100)
(100)
(100)
(100)
(100)
(100)
(100)
(001)
(001)
(001)
(001)
(001)
SUBSTRATE
(1̄012) α-Al2 O3

Figure 73

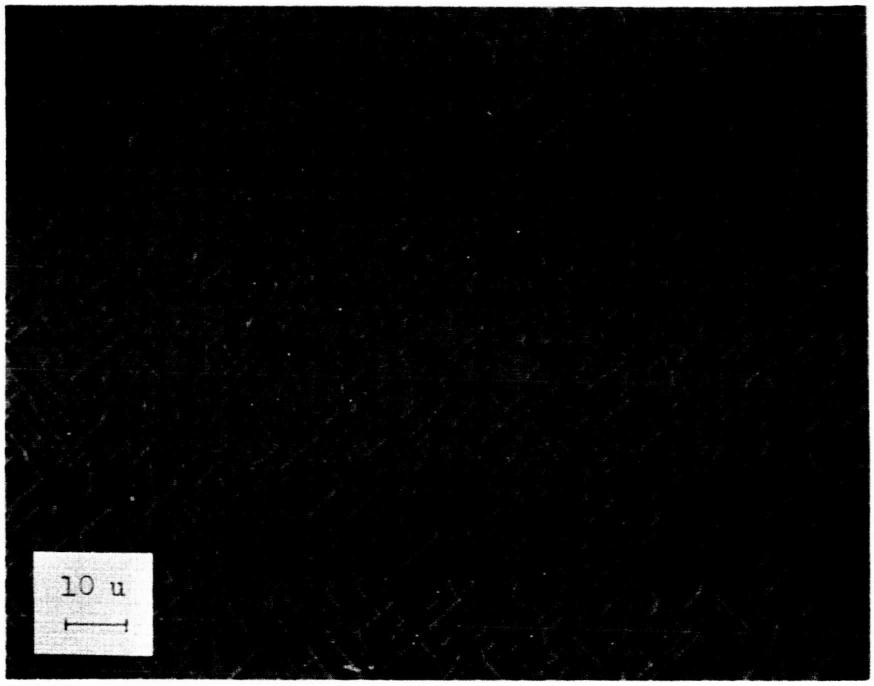
TABEL III

Sample No.	Resistivity ($\Omega\cdot cm$)	Carrier Concentration (cm^{-3})	Dopant	Hall Mobility ($cm^2/V\cdot sec.$ at 300°K)
MM 127	25.0	7.0×10^{14}	Boron	350
MM119	0.14	2.0×10^{17}	Boron	220
MM 141	0.05	1×10^{18}	Boron	150
MM 125	0.007	1.5×10^{19}	Boron	55
266 B	0.43	5.4×10^{16}	Aluminum	265
266 C	1.2	1.3×10^{16}	Aluminum	300
290 C	5.5	8.5×10^{16}	Aluminum	132
22 B	2.7	3.1×10^{16}	Aluminum	72
51 D	38.0	3.7×10^{15}	Aluminum	45
44 B	142.0	4×10^{15}	Aluminum	11

probably is the origin of the numerous scattering centers. For this reason the mobility at low temperature is affected predominantly by defect center scattering in addition to the normal impurity scattering due to the ionized impurities.

One would expect that the translation boundaries exhibited a much lower resistance to a chemical etch than the surrounding single crystal silicon material. A result of an etch study is illustrated in Figure 74. The photograph shows a polished and etched silicon film on (100) oriented spinel where a pattern of lines intersect at right angles. The pattern verifies the hypothetical picture of Figure 73. Assuming that the dark lines indeed represent the translation boundaries, the single crystal areas would be between 1 and 10μ in transverse dimensions.

Although the growth parameters for most of the samples made with the SiH_4 process were practically the same, the electrical parameters varied over a considerable range. The reason for this spread is not well established, but it seems that the original nucleation is extremely sensitive to even a minute variation of one or more of the many experimental parameters, which are: precision of crystallographic orientation and crystalline perfection of the substrate, molten salt or gas etch of the sapphire, pedestal temperature, hydrogen flow rate and flow pattern, concentration of SiH_4, and the geometry of the reaction tube. More investigations are necessary in order to establish a still better reproducibility of the process.



(100) Spinel with Polished and Etched Silicon Film Showing Four-Fold Symmetry.